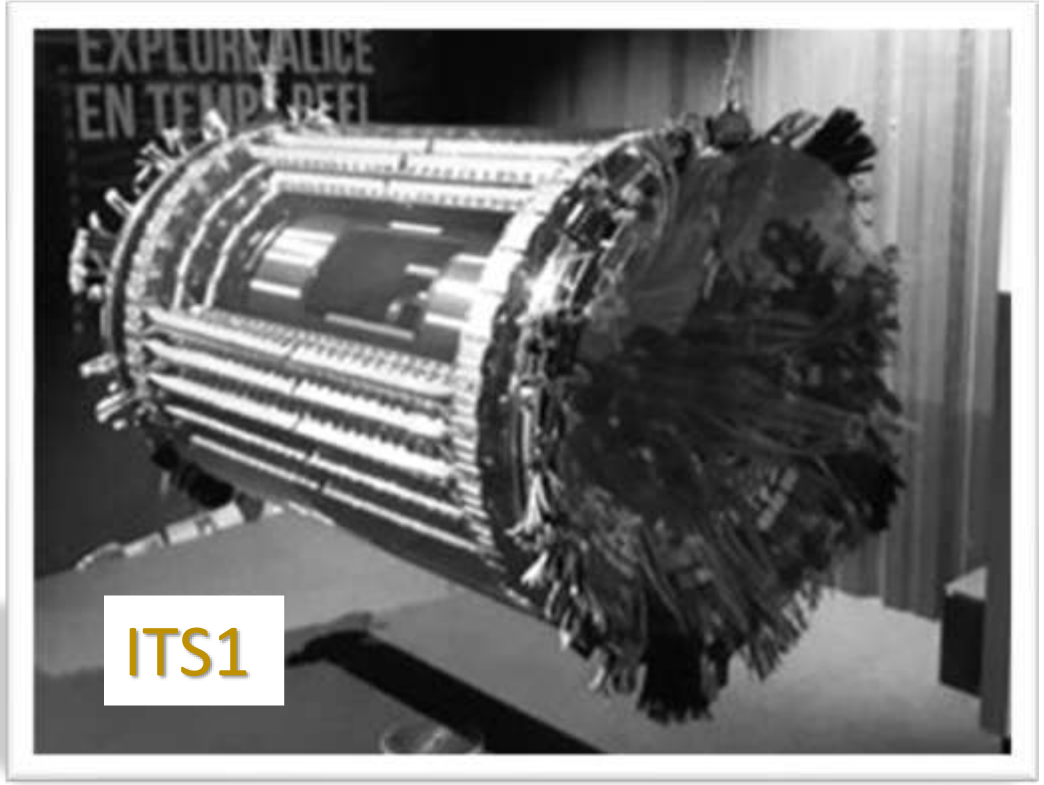
UNIVERSITY OF LIVERPOOL

ALICE

首届ALICE实验与重离子物理讲习班

The 1st ALICE Experiment and Heavy-Ion Physics School



ITS2

ALICE Inner Tracking System 2:

From Design and Construction to Run 3 Performance

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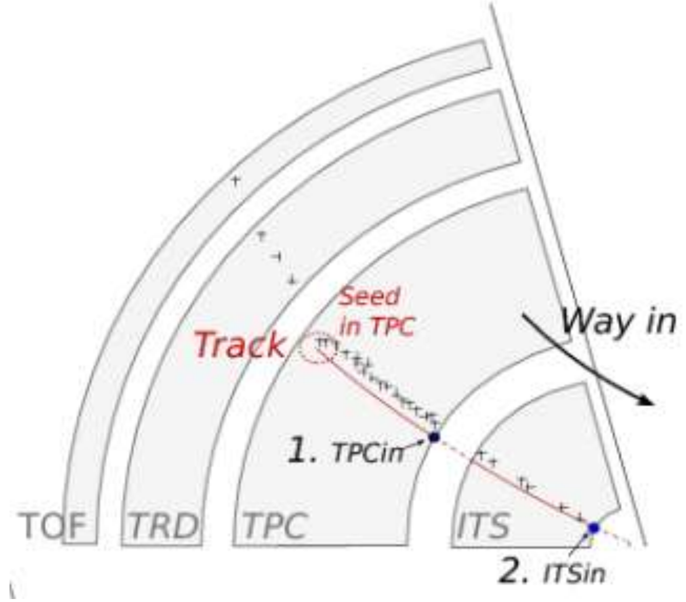
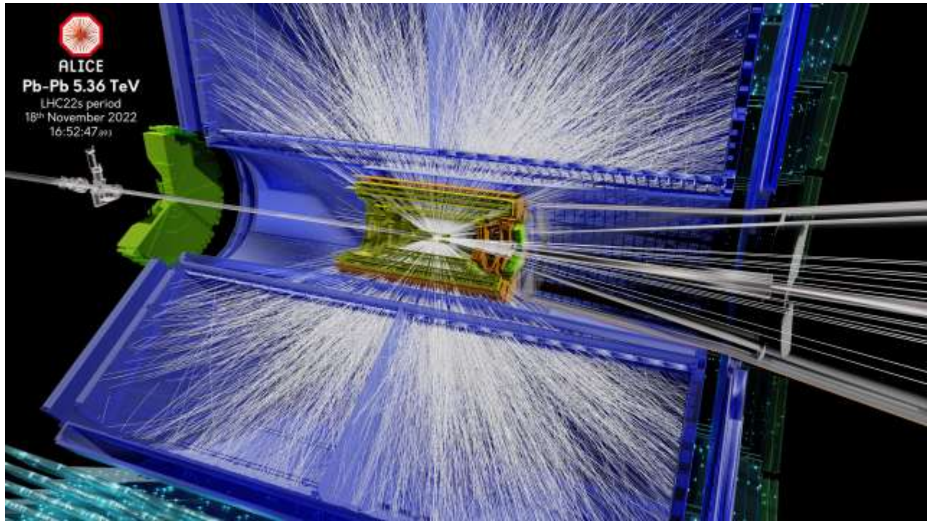
Tracking and vertexing in a high-energy collider experiment

- The **tracking system** reconstructs the trajectories of charged particles through the detector volume
- From track curvature in the magnetic field, we measure **momentum**; from intersection points, we locate **vertices**
- Precise **vertex reconstruction** is crucial for identifying **short-lived particles** (e.g. charm and beauty hadrons)
- Accurate tracking underpins nearly all physics analyses
  - Secondary-vertex reconstruction
  - Matching to other tracking and PID detectors (TPC, TOF, TRD)
- In ALICE, the ITS forms the **innermost part** of the tracking system — closest to the interaction point





Tracking Performance Determinants

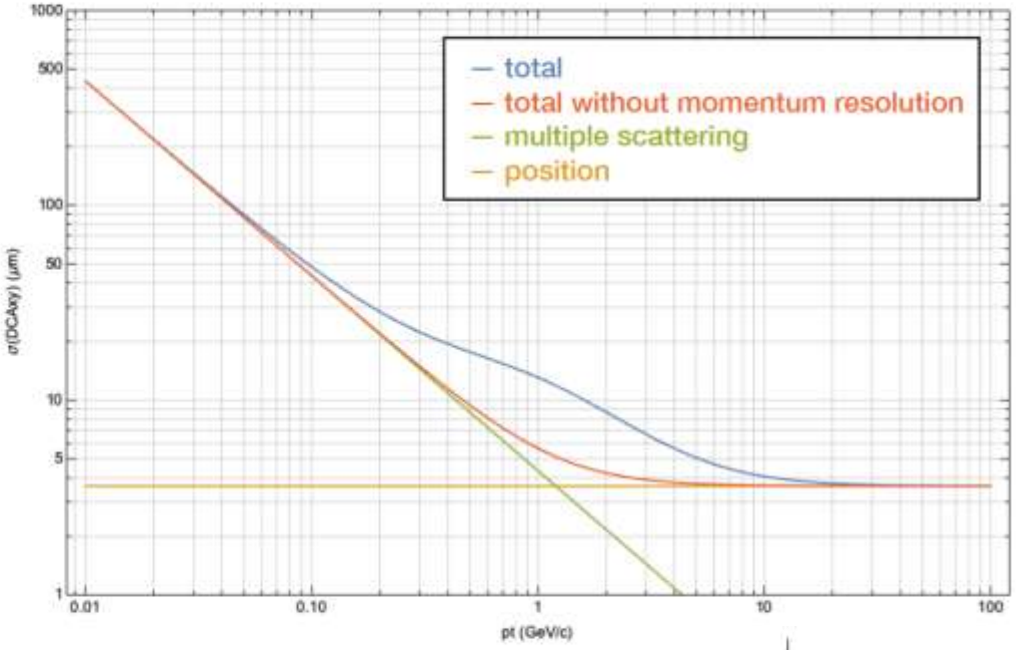
Limit	Momentum	Pointing
	$\frac{\Delta p_t}{p_t}$	$\Delta d_{0,xy}$
sensor resolution	$\propto \frac{\sigma p_t}{BL^2}$	$\propto r_0 \sigma$
material budget	$\propto \frac{1}{\beta BL}\sqrt{x/X_0}$	$\propto \frac{r_0}{\beta p_t}\sqrt{x/X_0}$

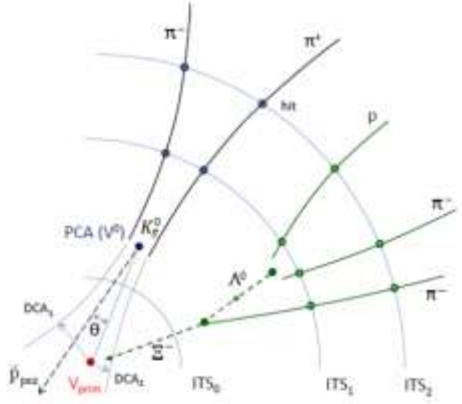
Key tracking and vertexing performance figures

- Impact-parameter resolution (pointing resolution)
- Momentum resolution
- Tracking efficiency
- Readout rate

Main contributors

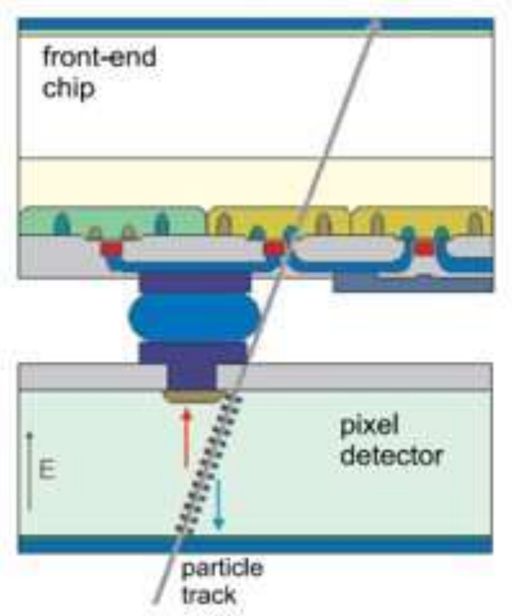
- Material budget (x/X_0): thickness of matter traversed, expressed as a fraction of the radiation length
  - Dominates at low p_T through multiple scattering
- Detector geometry: inner radius (r_0) and lever arm (L)
  - Smaller r_0 improves vertexing; longer L improves momentum resolution
- Intrinsic hit precision (σ): spatial resolution
  - Dominates at high p_T
- Intrinsic sensor detection efficiency

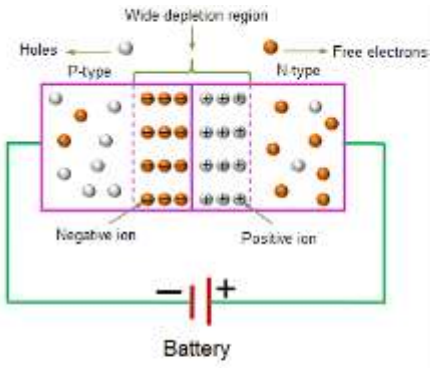


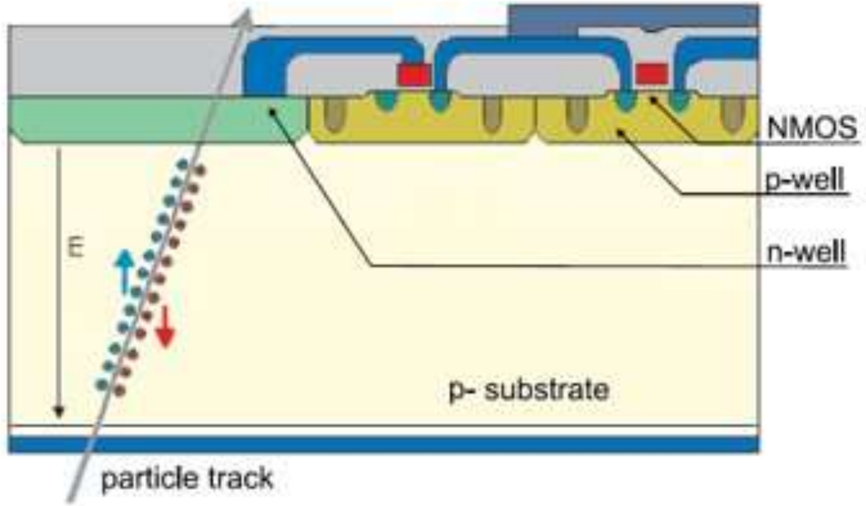


•**Pointing resolution:** the distance of closest approach (DCA) between the extrapolated particle trajectory and the reconstructed primary interaction vertex
•**σ:** intrinsic single-point precision (depends on pixel pitch and cluster size)
•**B:** magnetic field strength (0.5 T in ALICE)
•**L:** lever arm (radial distance between innermost and outermost hits)
•**r_0:** radius of the first measurement layer
•**x/X_0:** material thickness in units of radiation length

Pixel detector – hybrid vs monolithic







Hybrid

- 2 different chips: charge collection sensor + readout ASIC (application-specific integrated circuit)
- Large majority of presently installed systems – mature technology
- Full depletion – radiation hard
- 100 % fill factor can be achieved easily

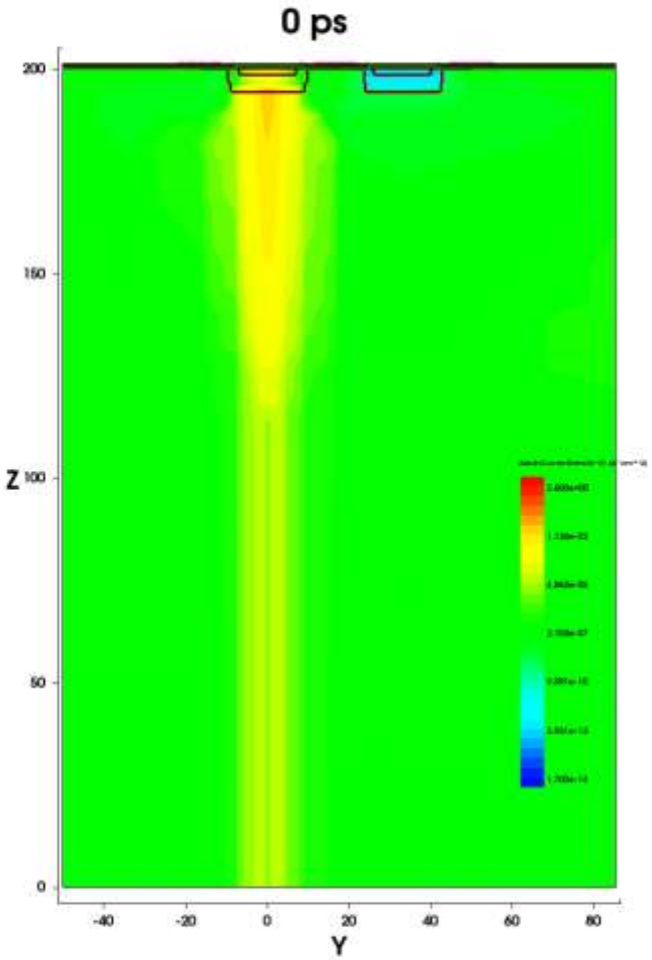
Monolithic active pixel sensor (MAPS)

- Commercial CMOS technology → lower price per unit area
- Can be thinned to tens of µm → material budget reduced
- Challenges
  - Radiation hardness: full depletion is not straightforward
  - Detection efficiency and fill factor
    - Electronics integrated into the same chip

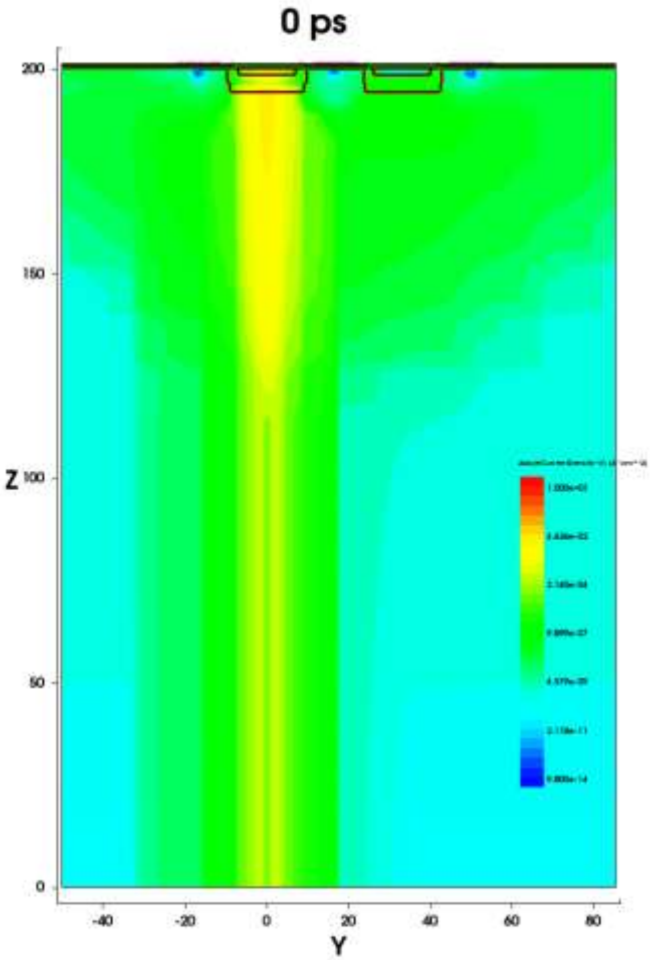
ITS2 chose this approach

Charge collection example

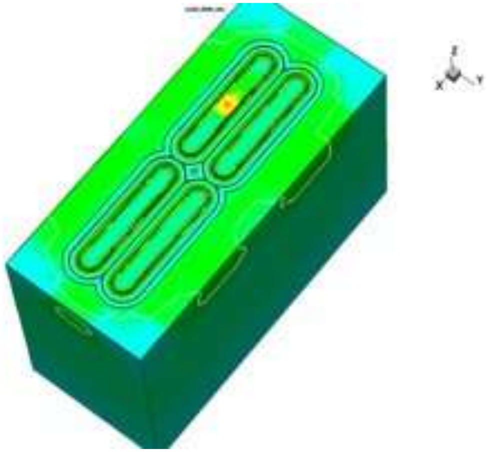
Impinging particle

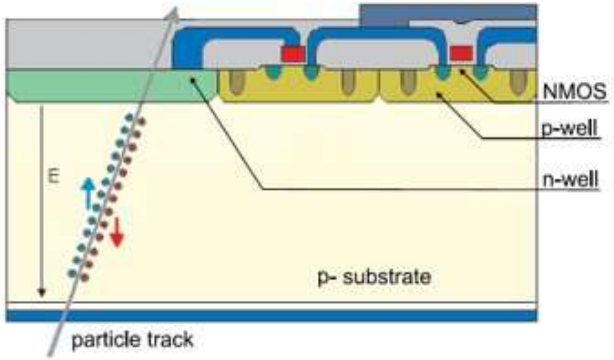


Electron



Hole

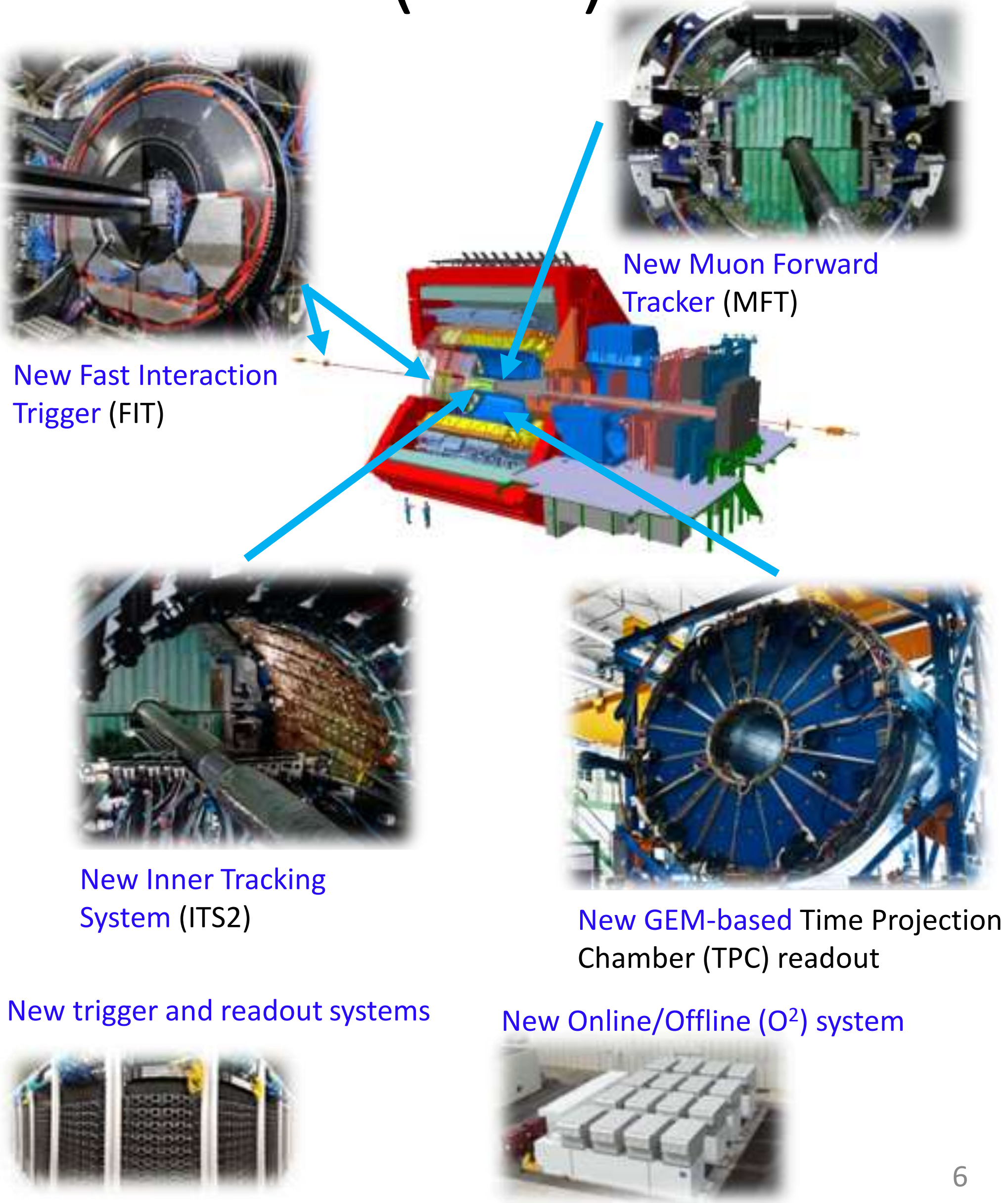




- Electrons in depletion region drift towards the charge collection n-well
- Holes are swept out towards bottom

ALICE upgrades in Long Shutdown 2 (LS2)

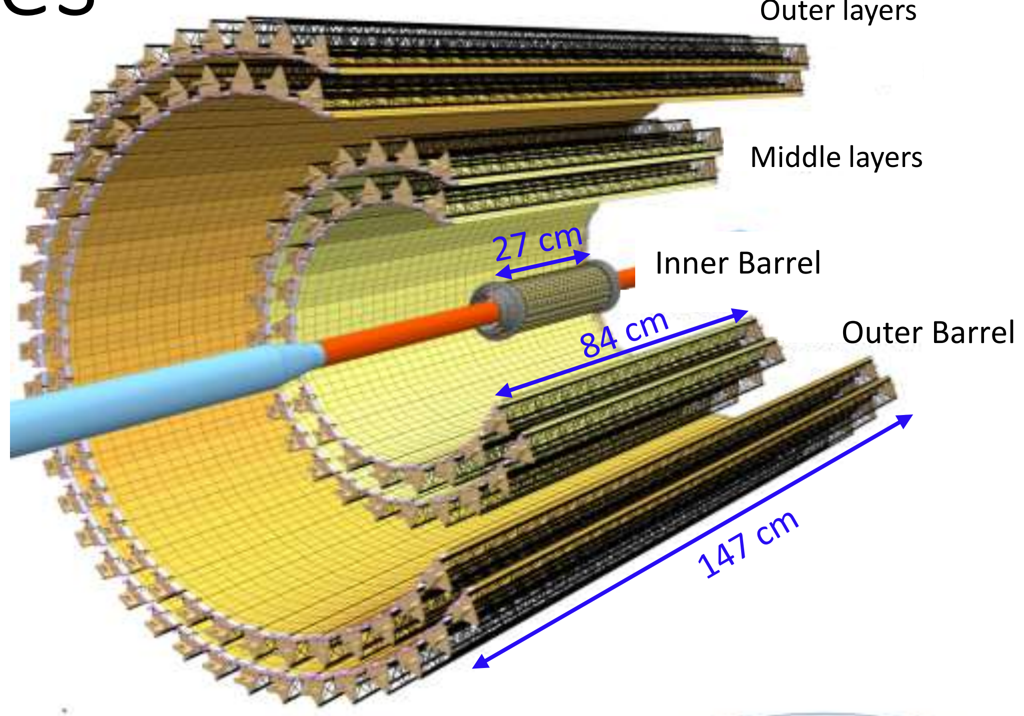
- Major upgrades completed for ALICE during LHC LS2 (2019 - 2021)
- Motivation
  - High-precision measurements of rare probes at low p_T
    - Cannot be selected by hardware trigger
    - Need to record large minimum-bias data sample → read out all Pb-Pb interactions up to the maximum collision rate of 50 kHz
- Goal
  - Pb-Pb integrated luminosity > 10 nb^{-1} in Run 3 and Run 4 (plus pp, pA and O-O data) → gain factor 100 in statistics for minimum-bias sample with respect to Run 1 and Run 2
  - Improved vertex reconstruction and tracking capabilities
- Strategy
  - New ITS, MFT, FIT and TPC readout chambers
  - New readout of most detectors and new trigger system
  - New integrated Online-Offline system (O^2)



ALICE upgrades during the LHC Long Shutdown 2, JINST 19 P05062

ITS2 objectives and challenges

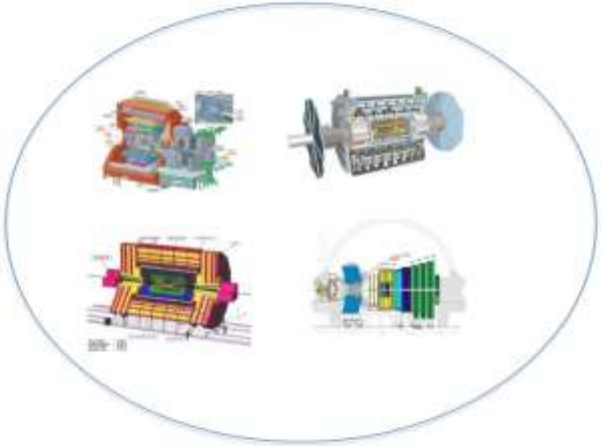
- Improve impact parameter resolution by a factor of ~3 in rϕ and factor ~5 in z at p_T = 500 MeV/c
  - Get closer to IP: 39 mm → 23 mm
  - Reduce material budget → lower multiple scattering
    - 1.14% X_0 → 0.36% X_0 per layer (inner layers)
  - Reduce pixel size: 50 x 425 μm^2 → 29 x 27 μm^2
- Improve tracking efficiency and p_T resolution at low p_T
  - Increase number of track points: 6 → 7 layers
- Fast readout
  - Detector readout rates up to 100 kHz (Pb-Pb, was 1 kHz for ITS1) and 400 kHz (pp)



192 staves
24120 chips
12.5 Giga pixels
10 m^2 active area

Largest pixel detector in High-Energy Physics

~ 10x readout channels



Technical Design Report for the Upgrade of the ALICE Inner Tracking System, J. Phys. G: Nucl. Part. Phys. 41 087002

ITS2 design and construction timeline

- 2012
- Dec ‘16
- May ‘19
- Dec ‘19
- Dec ‘20
- Jan ‘21
- May ‘21
- Oct ‘21
- Jul ‘22

Research & Development

- Conceptual Design Report: Sep ’12
- Technical Design Report: Nov ‘13

Detector construction and assembly

- ~72000 chips —> ~2600 Hybrid Integrated Circuits (HICs) —> ~280 staves
- > 10 production sites worldwide
- ~ 30 institutes involved

On-surface commissioning w/ final services

- 24/7 operation with ~200 shifters from ~30 institutes
- Calibration runs, cosmic muon data taking
- Key to spot potential issues early
- Valuable input for the planning of the installation
- Extremely valuable experience operating the detector

Installation

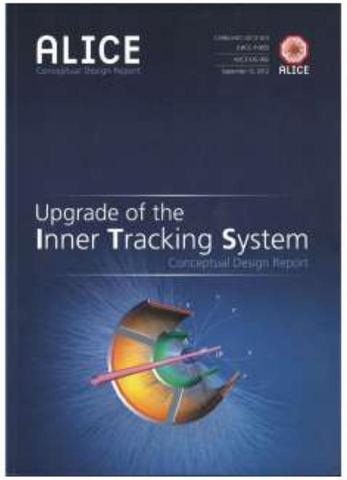
- Services installation in the cavern
- Outer Barrel installation
- Inner Barrel installation

On-site standalone and global commissioning

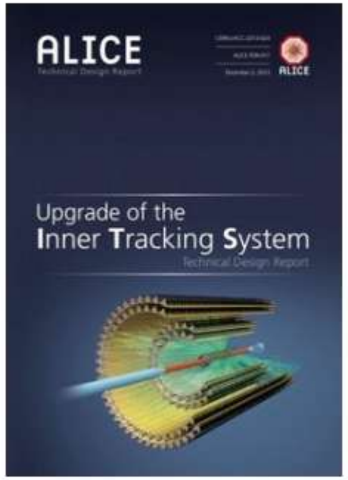
- Detector verification
- System integration

Pilot beam test

First physics collisions at top energy in Run 3!

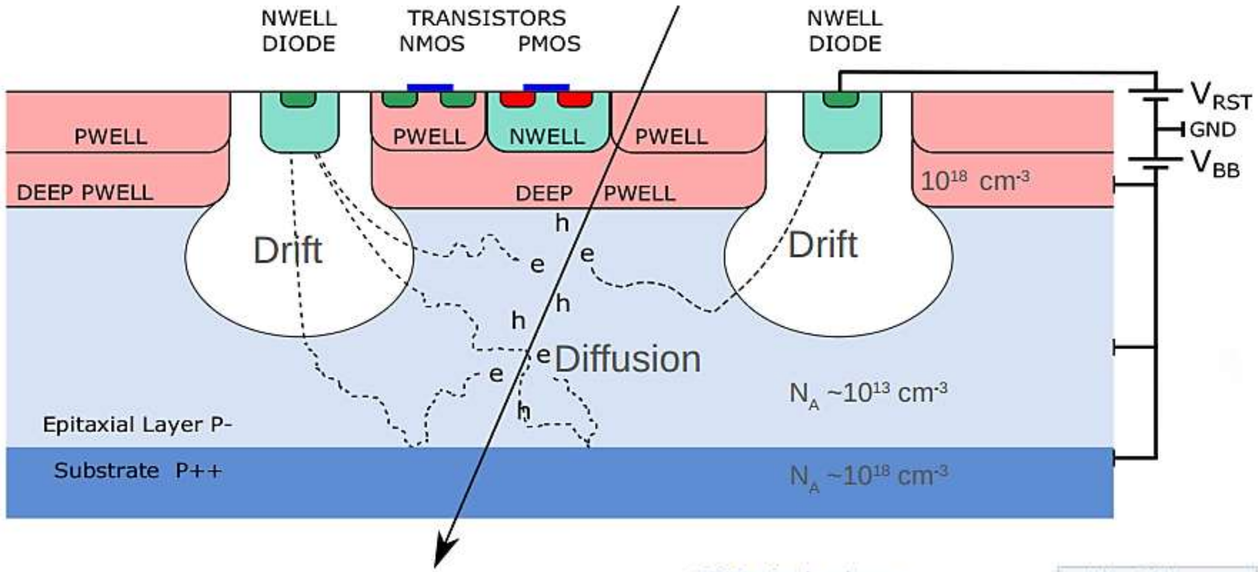


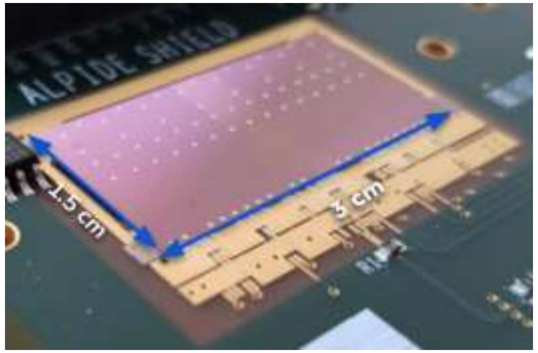
Conceptual Design Report

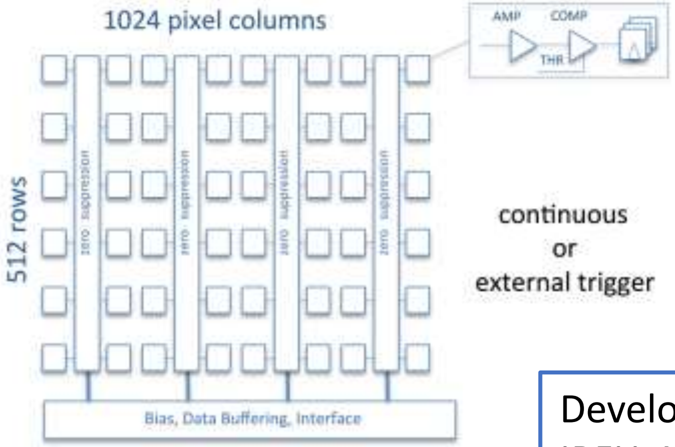


Technical Design Report

ALPIDE: **AL**ICE **PI**xel **DE**tector







ALPIDE technology features:

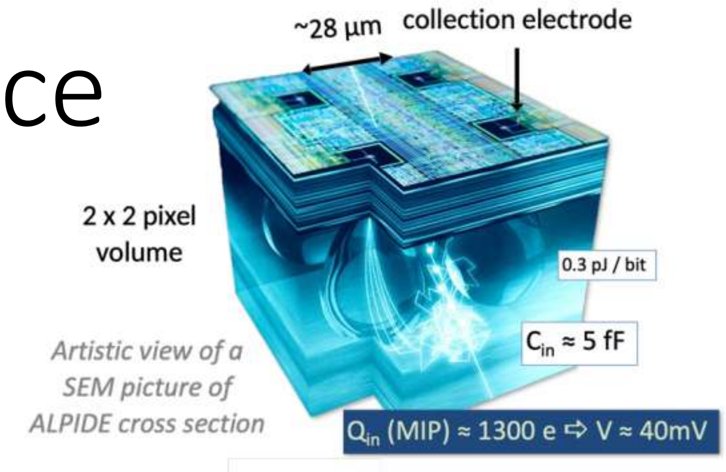
- TowerJazz 180 nm CiS Process
- Deep p-well implementation available → full CMOS
- High resistivity (>1 kΩ·cm), 25 µm thick, p-type epi-layer
- Possibility of reverse biasing (-6 V < V_{BB} < 0 V)
- Smaller charge collection diode
  → lower capacitance → higher signal-to-noise ratio
- Substrate can be thinned down

Sensor specification:

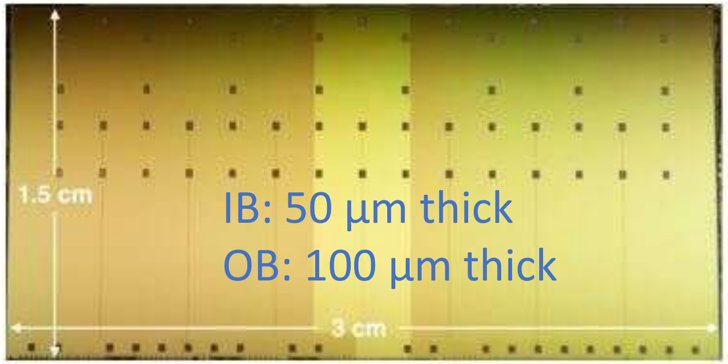
- Sensor size: 1.5 x 3 cm^2
- Number of pixels: 1024 x 512
- Pixel pitch: ~27 µm x 29 µm
- Priority Encoder Readout
- Low power consumption < 40 mW/cm^2
- Readout bandwidth up to 1.2 Gbit/s (IB) and 400 Mbit/s (OB)
- Continuous or triggered readout

Development effort involving **CCNU**, CERN, INFN (Torino, Cagliari), IPHC, IRFU, NIKHEF, YONSEI

ALPIDE requirements and performance



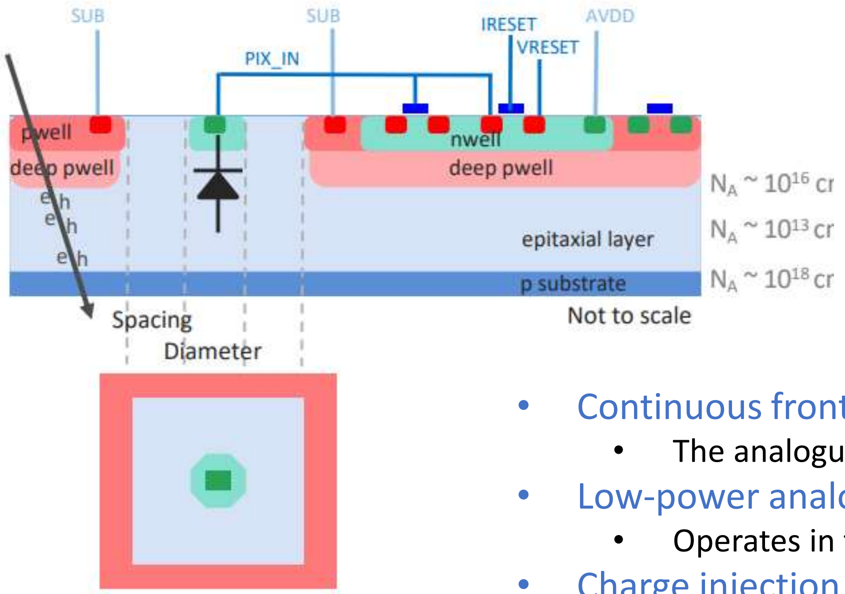
Parameter	Requirement	ALPIDE
Spatial resolution (μm)	≈ 5	≈ 5
Integration time (μs)	< 30	< 10
Fake-hit rate (/ pixel / event)	$< 10^{-6}$	$<< 10^{-6}$
Detection efficiency	> 99%	>>99%
Power consumption (mW / cm^2)	< 100	47.5 (IB) 35 (OB)
Total Ionising Dose (TID) (krad)	> 270 (IB) > 10 (OB)	OK
Non-Ionising Energy Loss (NIEL) (1 MeV n_{eq} / cm^2)	$> 1.7 \times 10^{12}$	OK

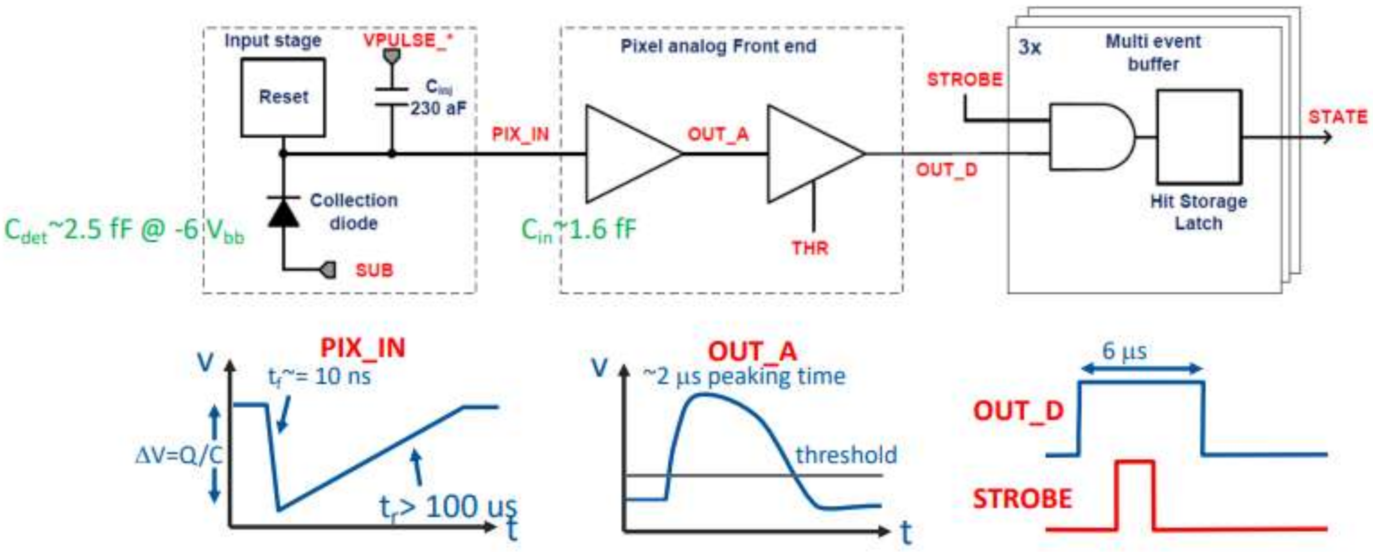


- > 70 k chips produced and tested
  - 24 k in operation on ITS2 + several other applications, e.g., sPHENIX MVTX (MAPS Vertex Detector)

Not technology limits but mostly design choices!

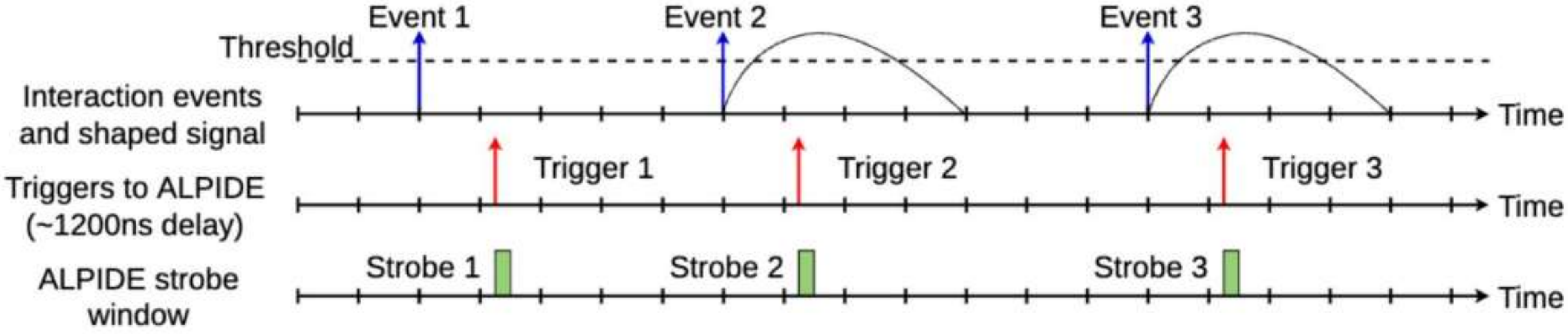
Pixel architecture



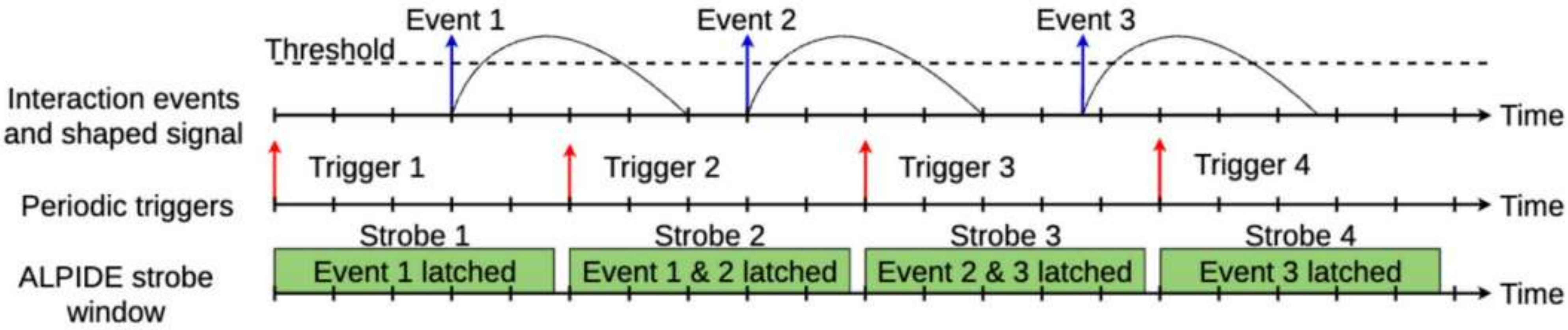


- Continuous front-end activity
  - The analogue front-end and discriminator remain continuously active to process incoming signals in real time
- Low-power analogue design
  - Operates in the weak inversion region, achieving ultra-low power consumption (~40 nW per pixel)
- Charge injection and testing
  - Each pixel includes test-pulse injection circuitry for calibration and verification
- Binary discrimination
  - A global threshold defines the discrimination level, producing a binary output pulse (OUT_D) for each hit
- In-pixel buffering
  - The digital pixel logic contains three hit-storage registers (multi-event buffer) to store hits
- Hit latching via Strobe
  - The Strobe signal latches discriminated hits into the next available register
- In-pixel masking
  - Each pixel incorporates masking logic to disable noisy or malfunctioning channels individually

ALPIDE readout modes



(a) Triggered mode



(b) Continuous mode

Charge generation and sharing in ALPIDE

Generated charge

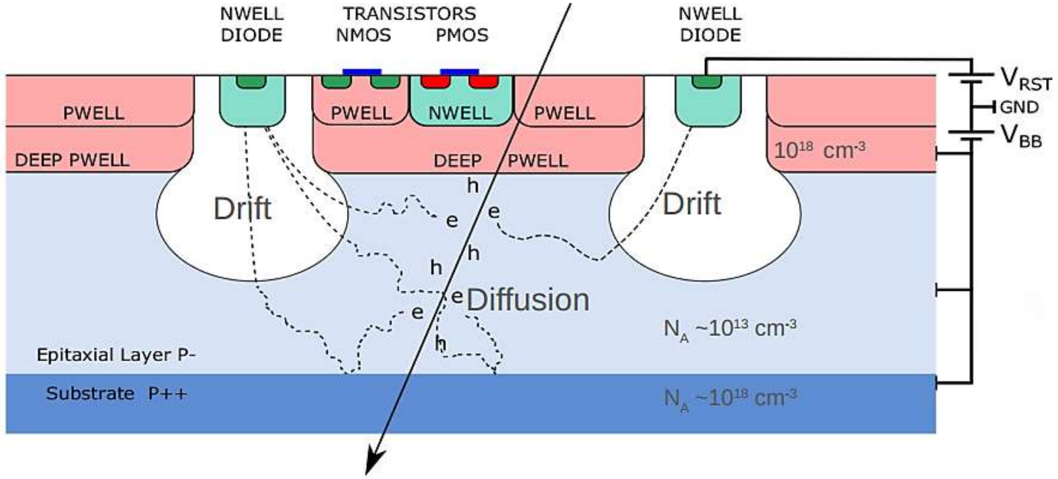
- A minimum-ionizing particle (MIP) creates about 60 e⁻/μm in silicon
- In the 25 μm epitaxial layer of ALPIDE → total signal ≈ 1500 e⁻ for a perpendicular track

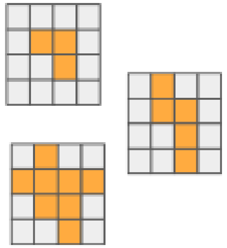
Charge sharing

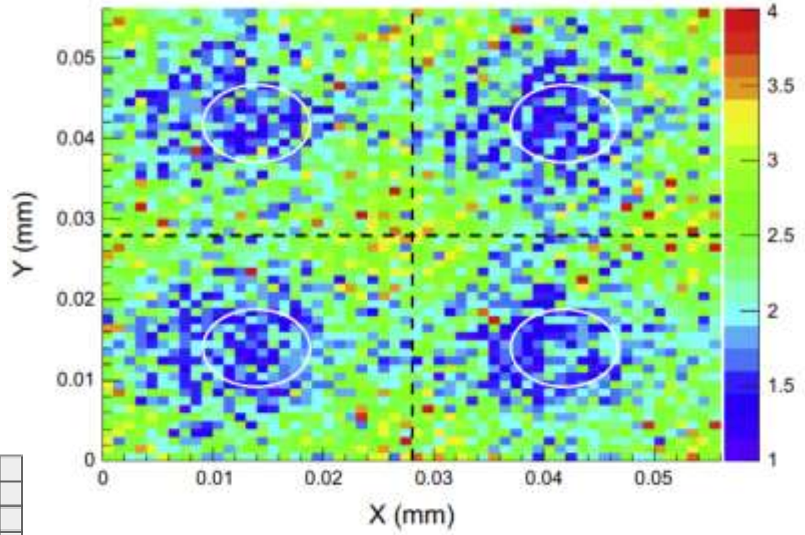
- Charge is not collected in a single pixel — electrons diffuse laterally, forming multi-pixel clusters
- Cluster size depends on impact point, field configuration, and sensor bias
- Minimum 15% (≈ 225 e⁻) of the generated charge reaches the seed pixel under diffusion-dominated conditions
- The collected fraction can increase to ~80 % when a reverse-substrate bias is applied (enhanced drift e-field)

Further effects

- Highly ionizing particles can deposit an order of magnitude more charge
- Inclined tracks traverse a longer path → generate more charge and exhibit larger clusters

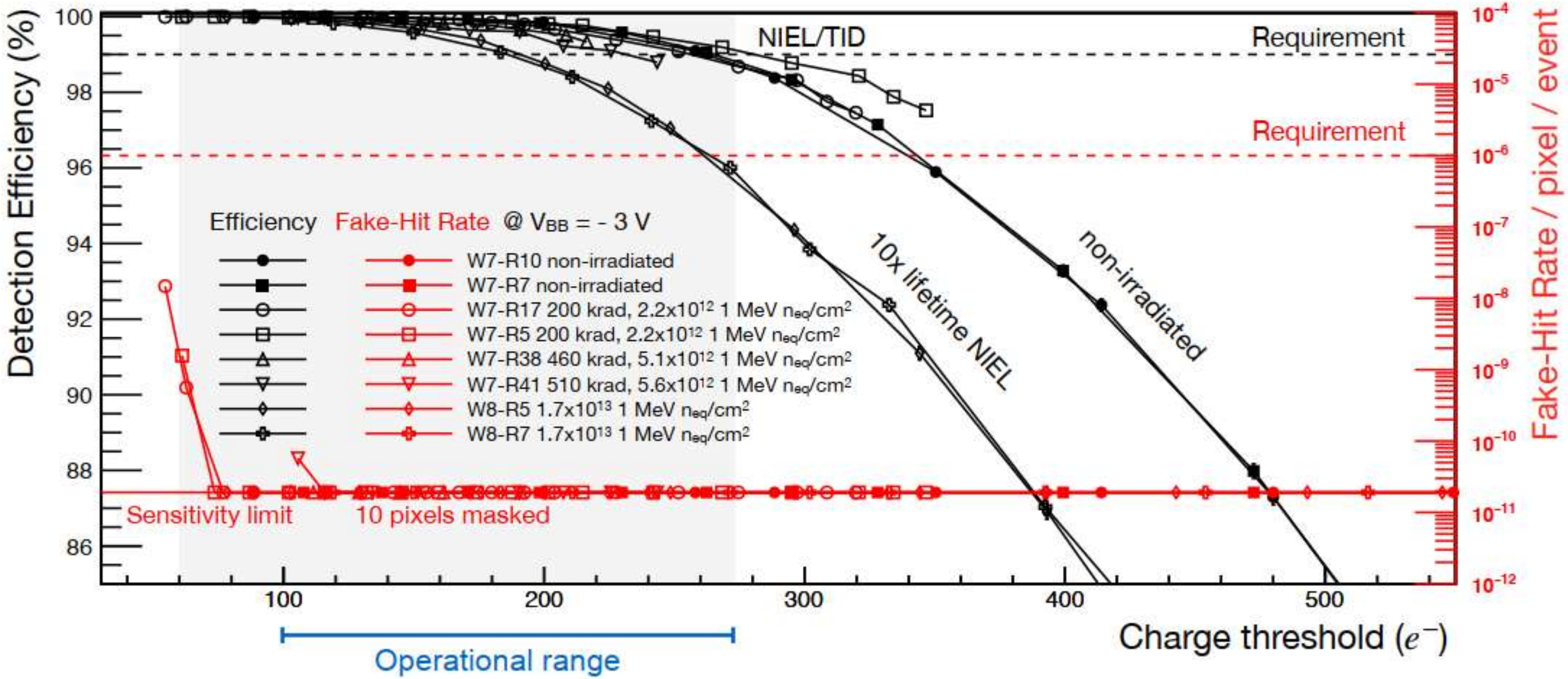






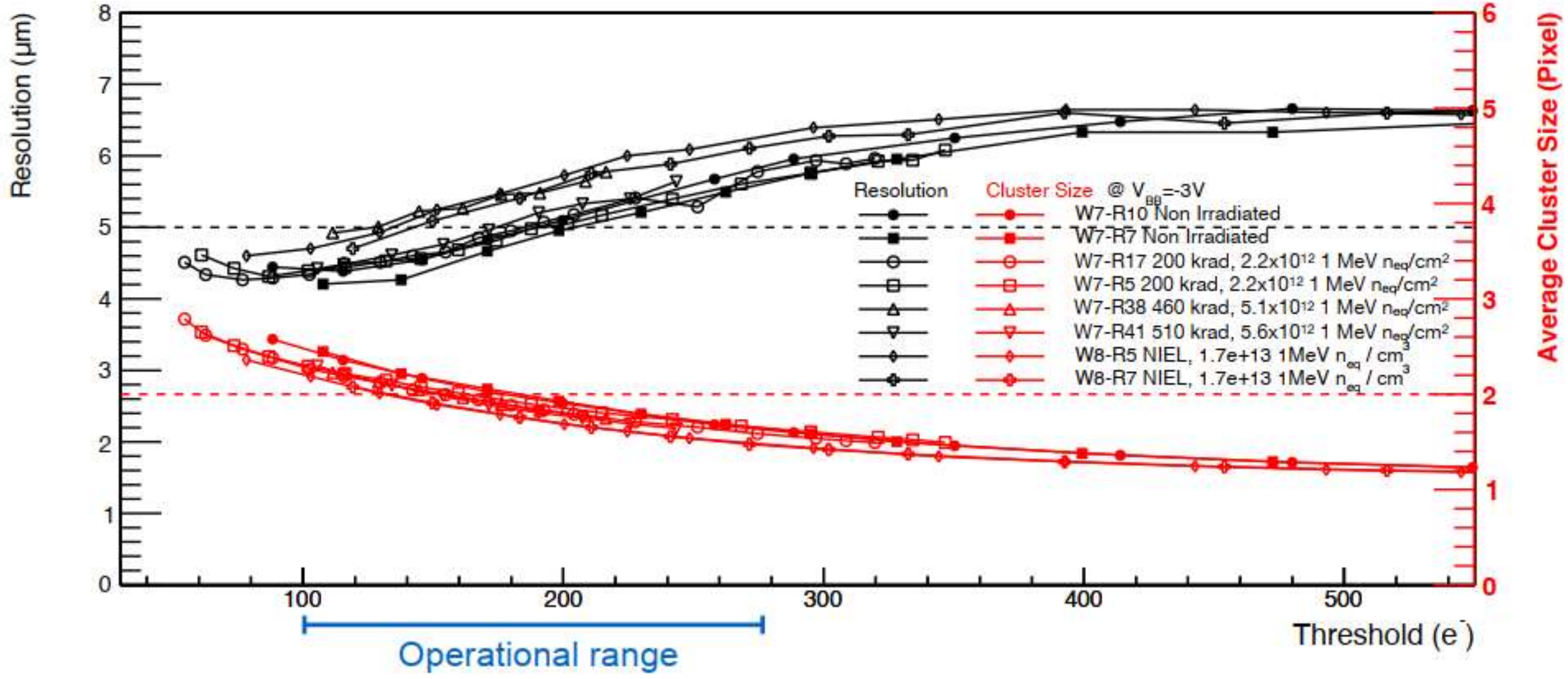
Avg. cluster size vs hit position

ALPIDE – detector efficiency and FHR



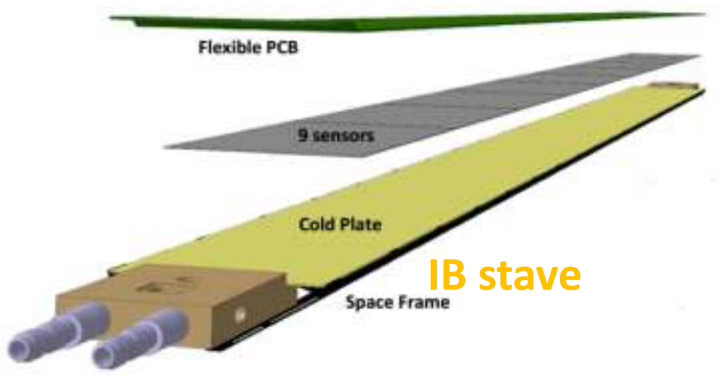
- Wide operational range achieved after exposing to the expected radiation load

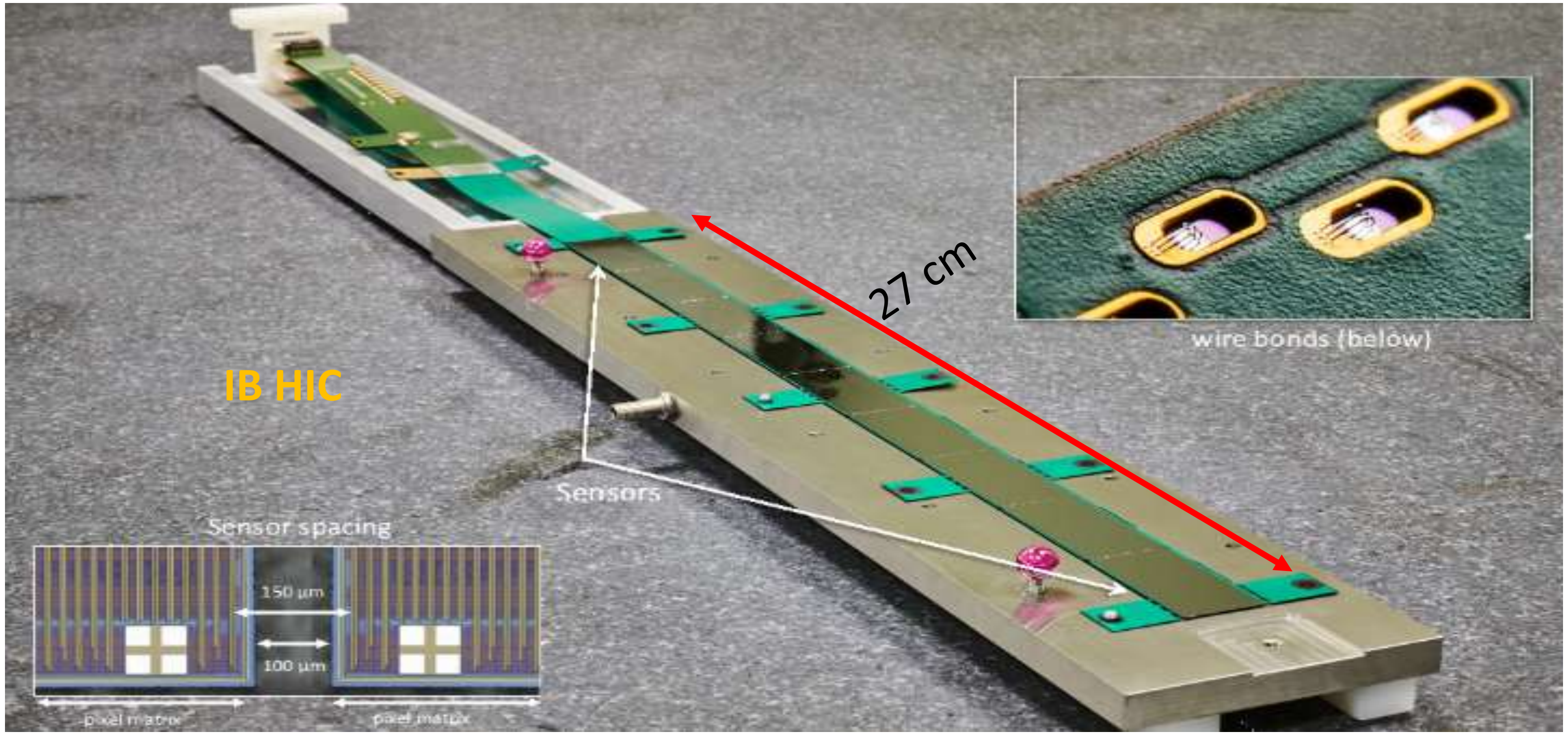
ALPIDE – cluster size and spatial resolution



- Spatial resolution of 4–5 μm, better than the 30 μm/√12 ≈ 8 μm baseline
  - Improved charge sharing notably enhances spatial resolution, though it also demands increased bandwidth

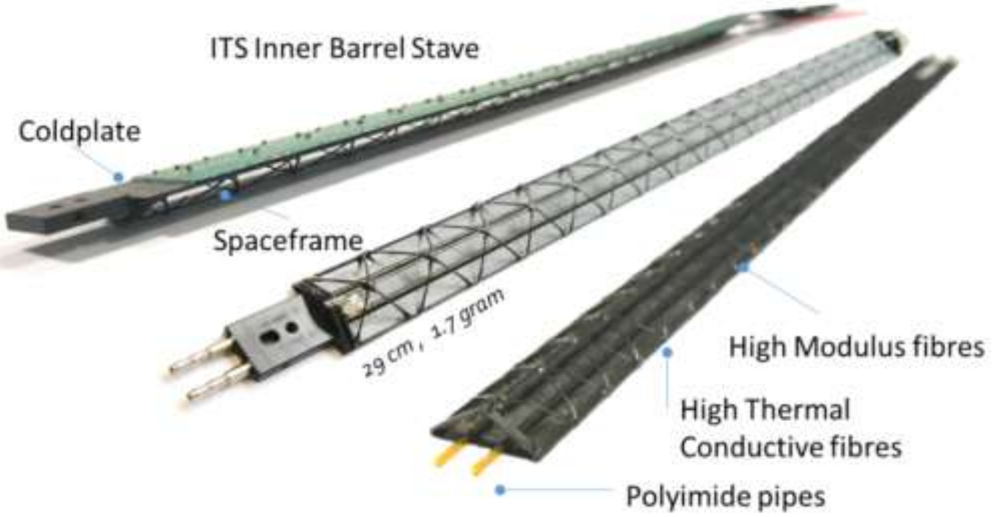
Inner Barrel

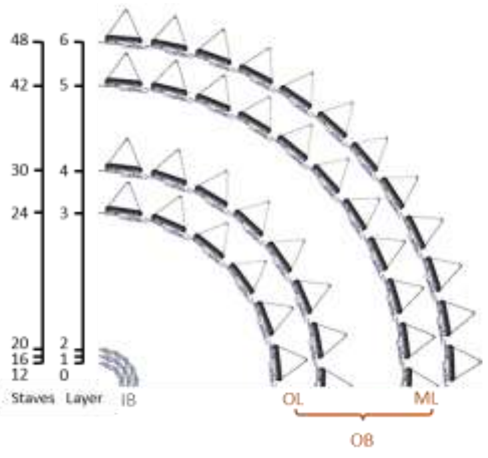




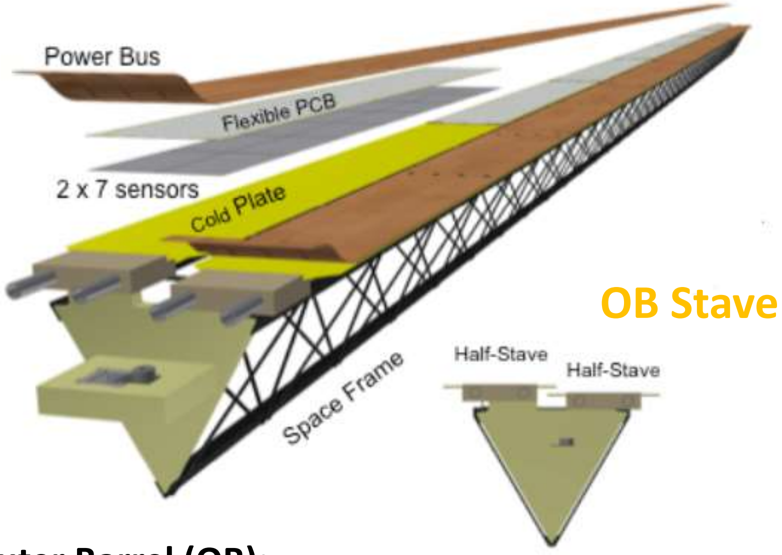
Inner Barrel (IB):

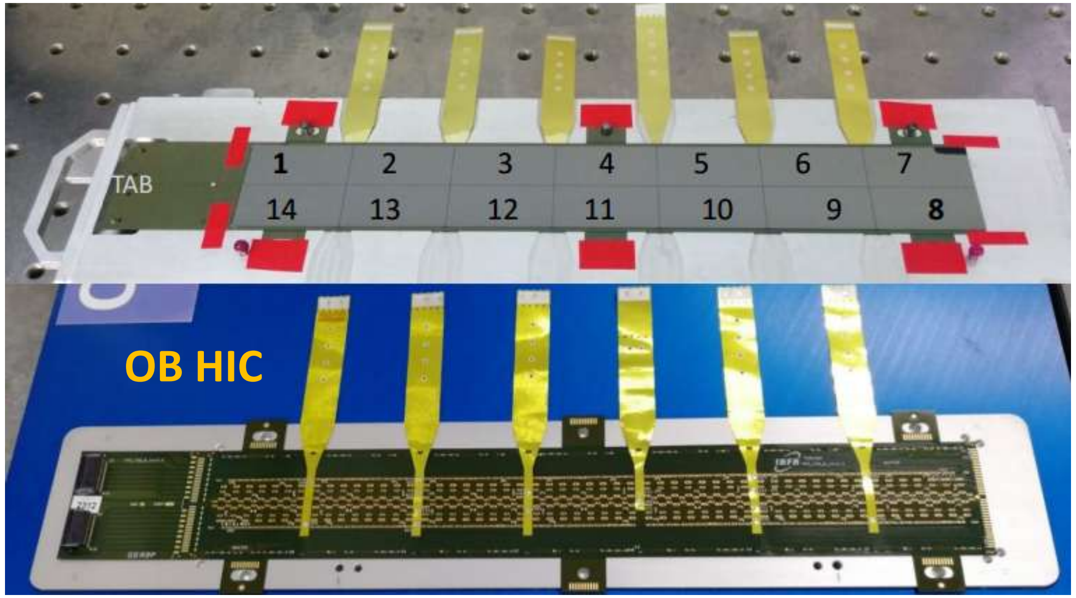
- Three layers
  - Layer0: 12 staves
  - Layer1: 16 staves
  - Layer2: 20 staves
- Hybrid Integrated Circuit (HIC): 9 sensors glued onto Al Flexible Printed Circuit (FPC)
- Wirebonds electrically connect FPC to chips
- Stave: a HIC glued onto a cold plate and space frame
- Each sensor is read out individually

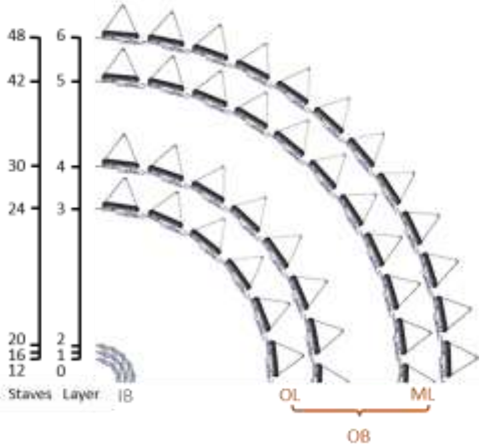


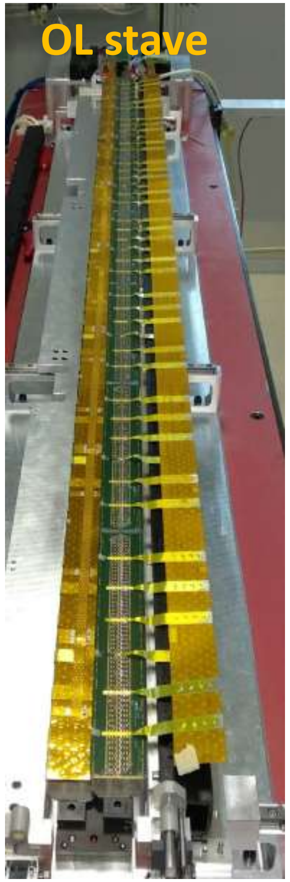


Outer Barrel





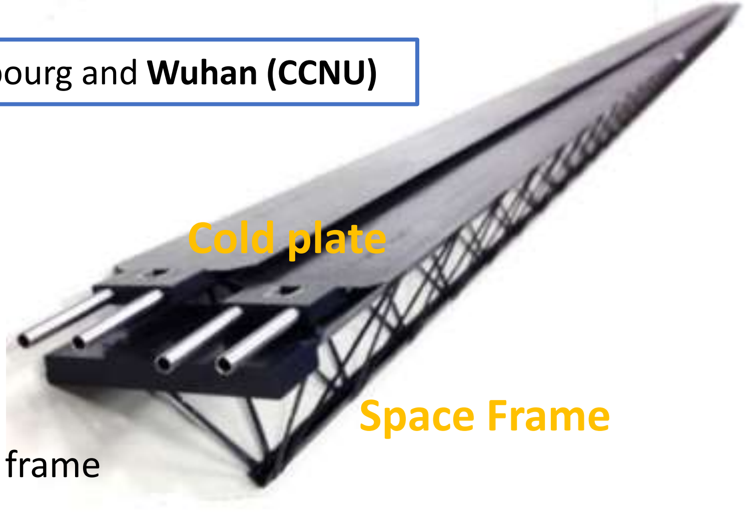




Outer Barrel (OB):

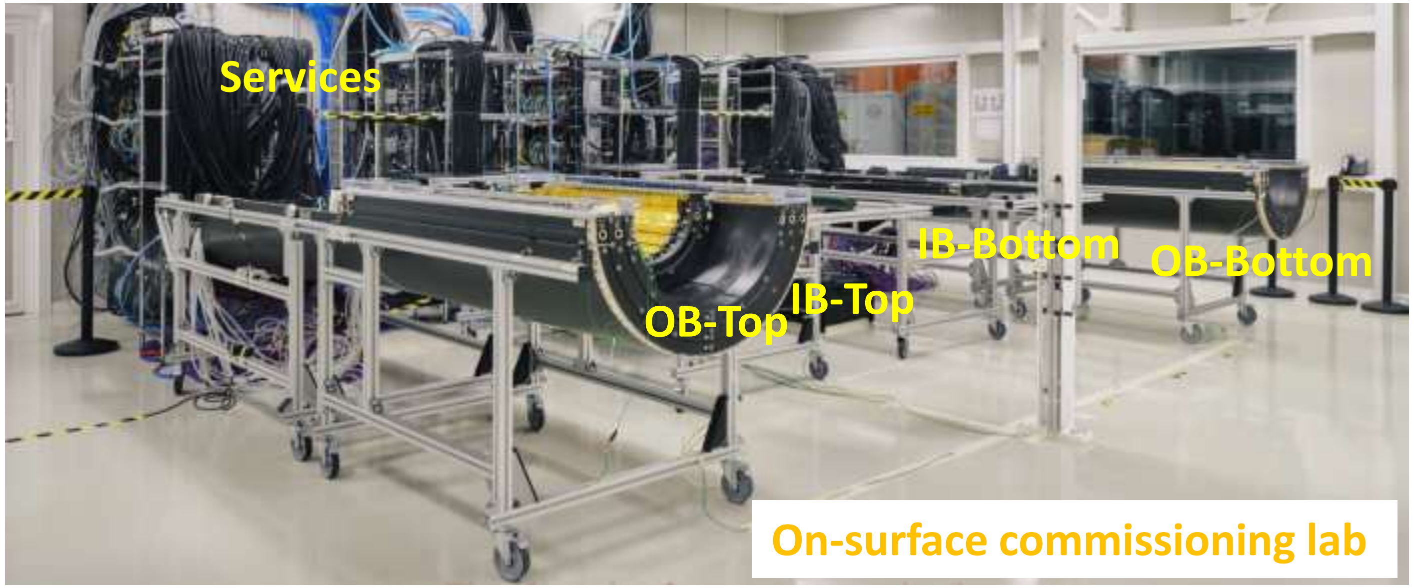
- Two Middle Layers (ML)
  - 24 + 30 staves
- Two Outer Layers (OL)
  - 42 + 48 staves
- OB HIC (module):
  - 7x2 sensors (2 rows) glued onto Cu FPC
  - Wirebonds electrically connect FPC to chips
  - Power delivered via 6 Al cross-cables soldered to the FPC
  - Data and control are transferred through 1 master chip per row
- OB stave:
  - 4x2 HICs (for ML) or 7x2 HICs (for OL) glued onto a cold plate and space frame

HIC assembly sites: Bari, Liverpool, Pusan/Inha, Strasbourg and **Wuhan (CCNU)**

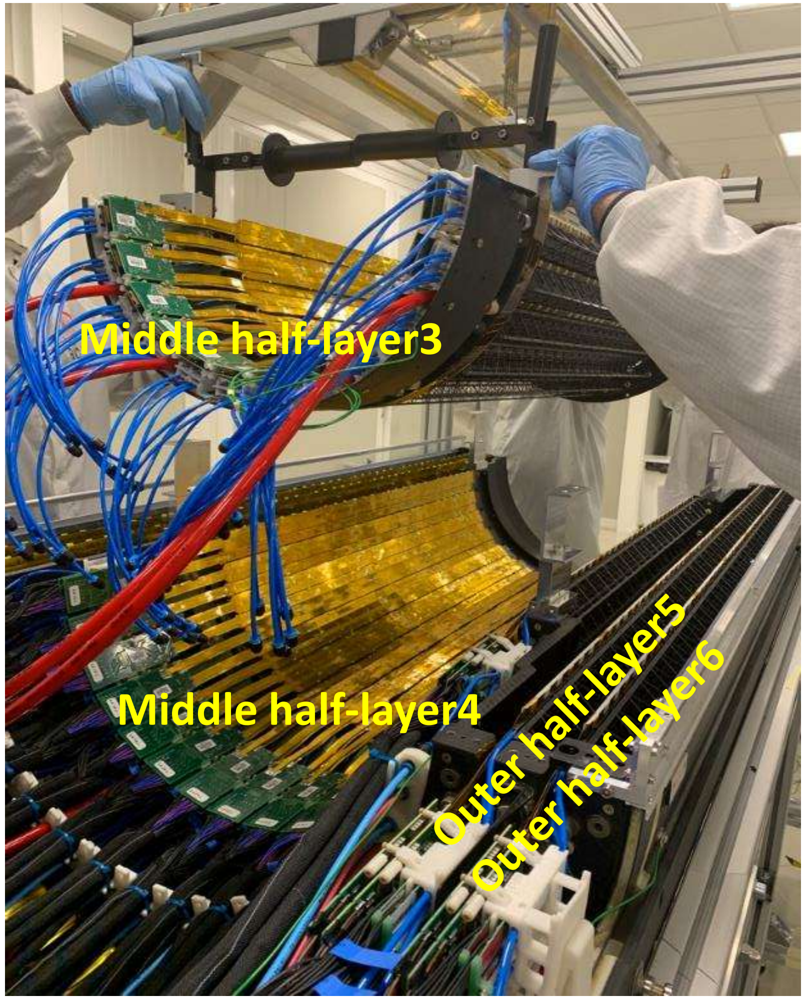


Layer and Barrel Assembly

Inner Barrel assembly



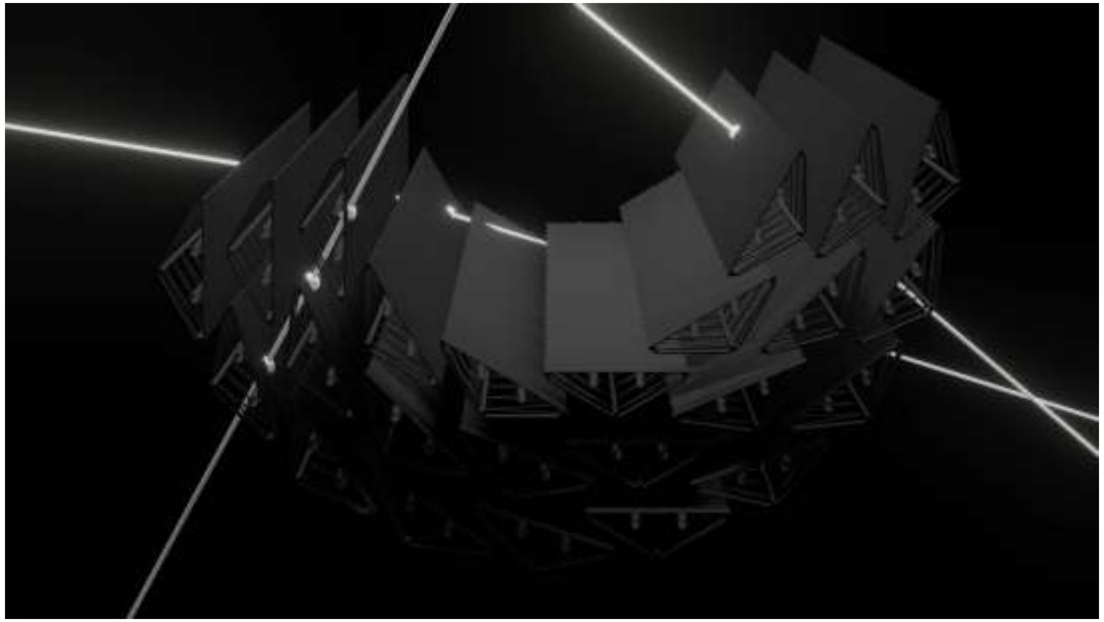
Outer Barrel assembly



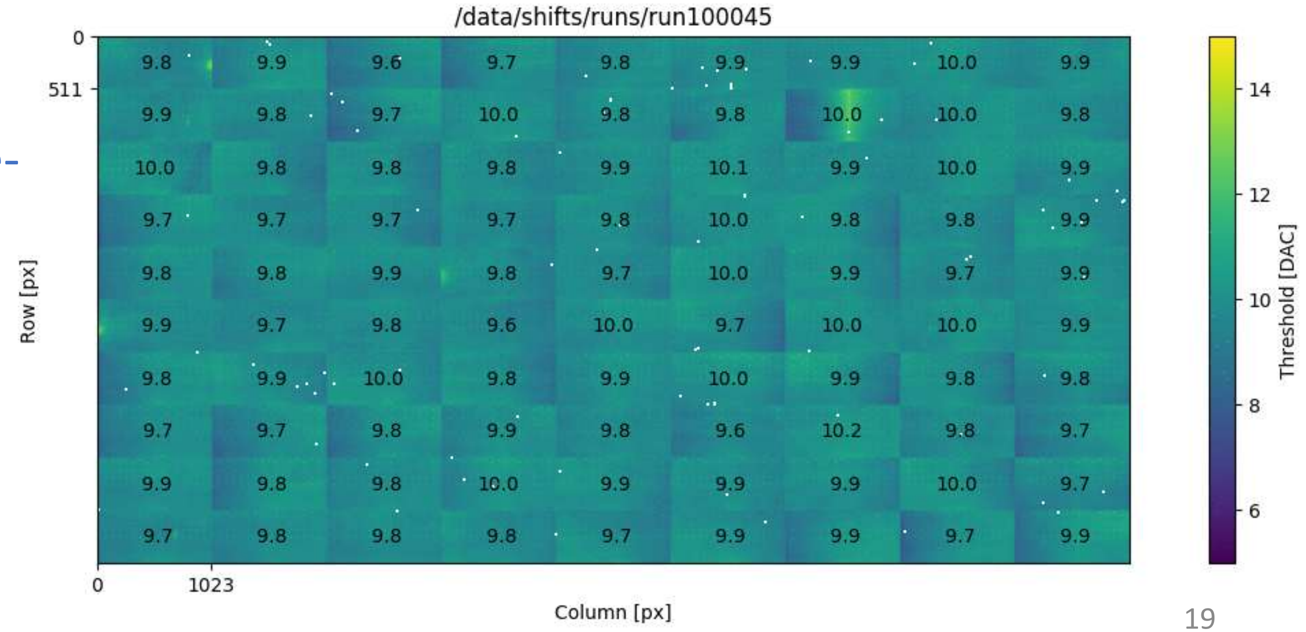
Detector fully assembled in Dec. 2019

On-surface commissioning

- Commissioning shifts 24/7 started in July 2019
- 3 daily slots with 2 shifters + 1 shifter leader
- Completed in December 2020
- Verification of detector performance and long stability of parameters
- Detector status monitoring: voltage, current and temperature monitoring
- Standalone data taking: threshold scans, fake-hit rate runs and readout tests
- Offline data quality control

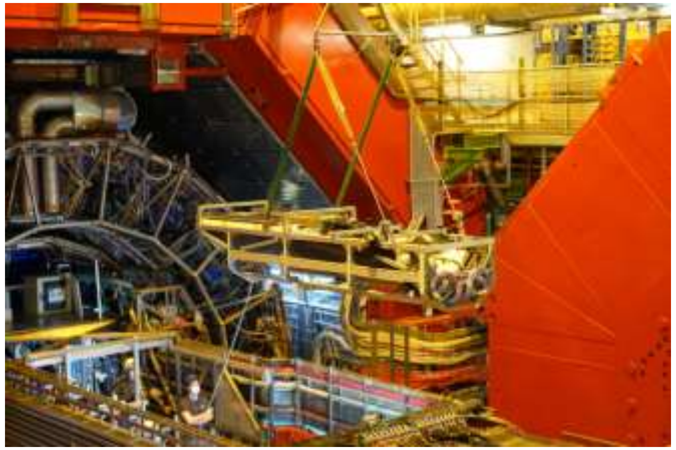


Reconstructed cosmic tracks



Threshold stability

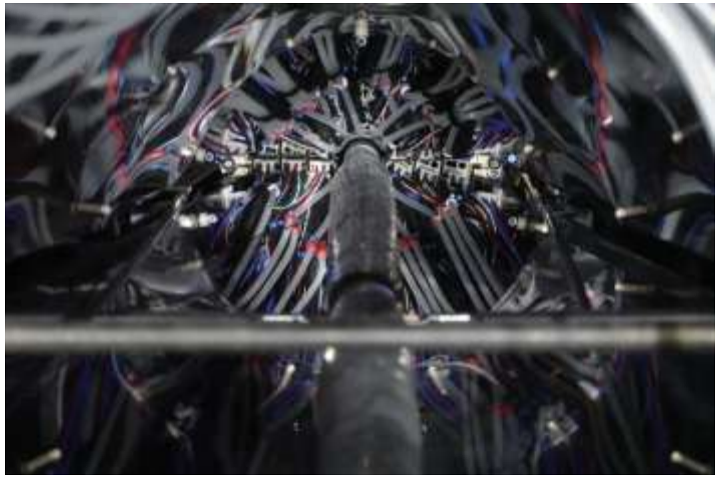
Installation



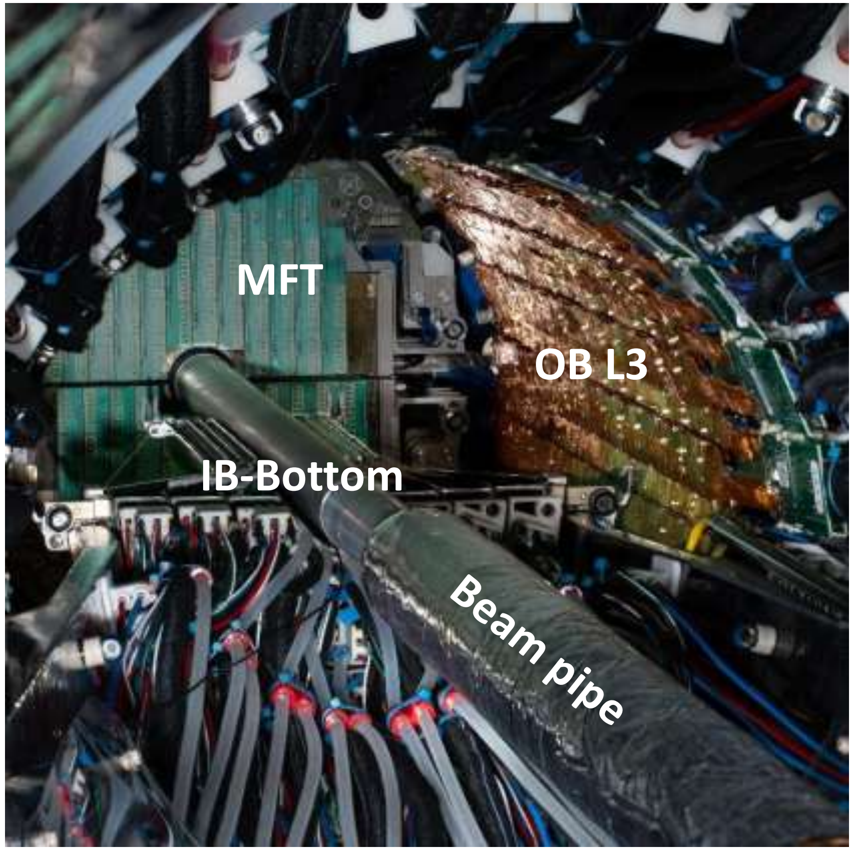
OB-Bottom being loaded to mini-frame

OB-Bottom being positioned

IB being installed



IB installed

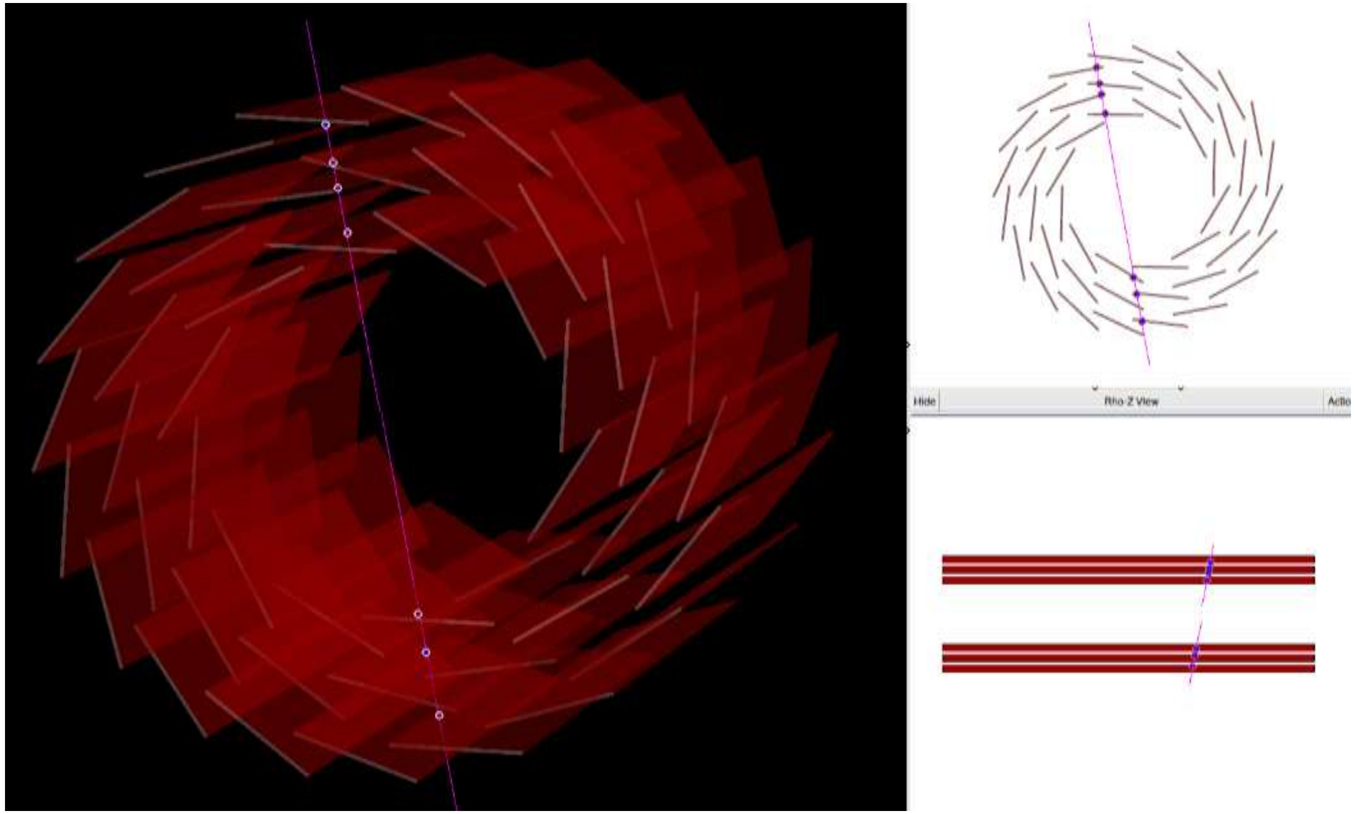


OB installation completed – mid March 2021
IB installation completed – mid May 2021

On-site commissioning

- Standalone (April – June 2021)
  - Similar shift configuration as the on-surface commissioning
  - Central system integration
  - Detector status monitoring + expert tests
  - Detector validated after the installation in the cavern
- Global (July – December 2021)
  - Shifts organized by ALICE + ITS on-call shifts
  - Central system integration/benchmarking
  - Validation/finalization of the online data processing/monitoring chain
  - Detector alignment + calibration
  - Technical + physics (cosmics + pilot beams, etc) runs

A cosmic track from the full IB



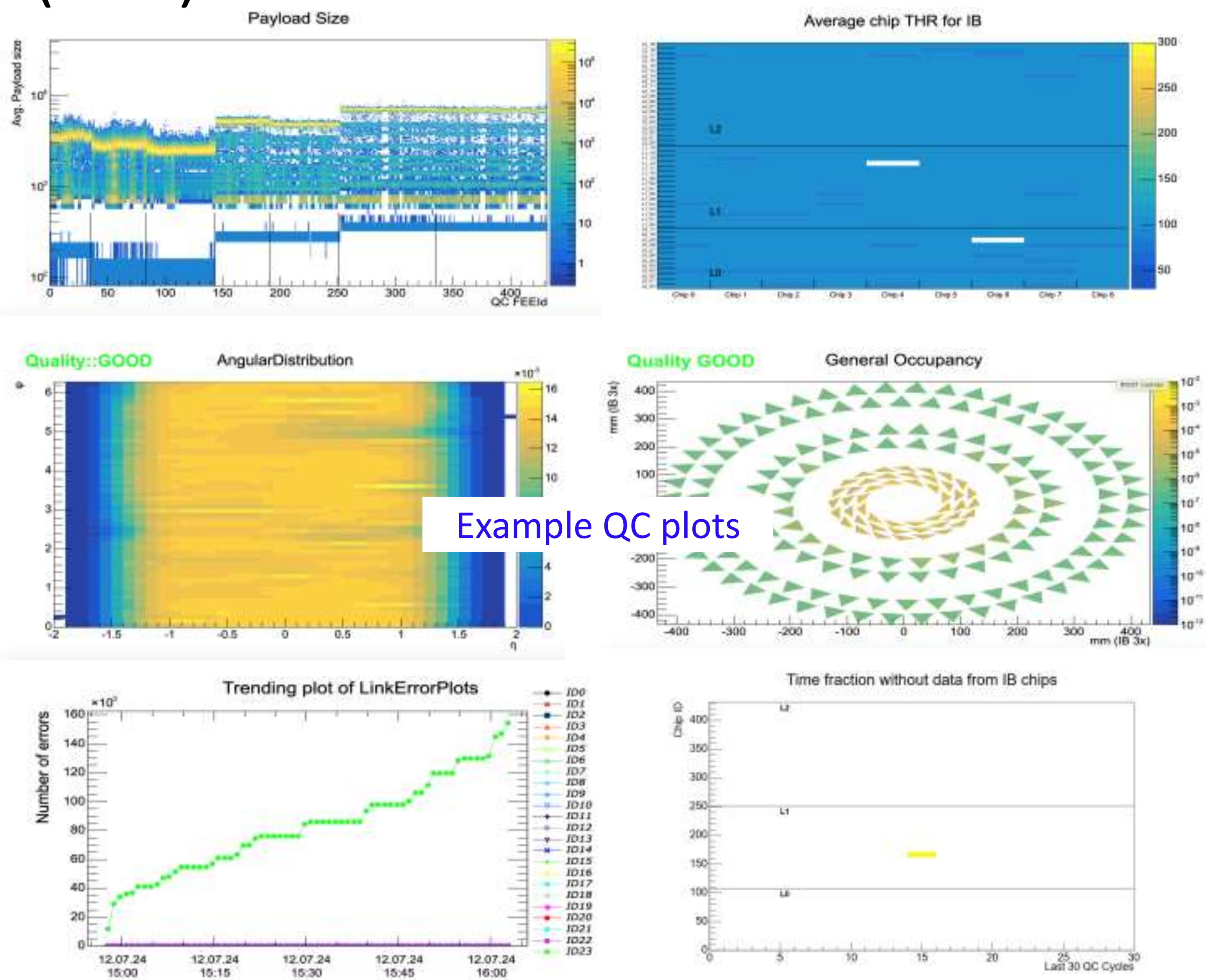
Data quality control (QC)

- Dedicated online tasks to monitor data quality in data taking and calibration scans
  - Front-end electronics: data integrity check using diagnostic information in raw data
  - Occupancy: detector occupancy
  - Cluster: cluster size, topology, etc.
  - Track: track multiplicity, angular distribution, clusters attached to tracks, etc.
  - Decoding errors: data corruption
  - Chip status: missing chips in data taking
  - Threshold: threshold, noise, dead pixels, etc.

- Time-dependent quality checks for both online and offline reconstruction → bad data during a run can be excluded during physics analysis

- Post-processing (online and offline): analysis and trending of QC plots (run by run)

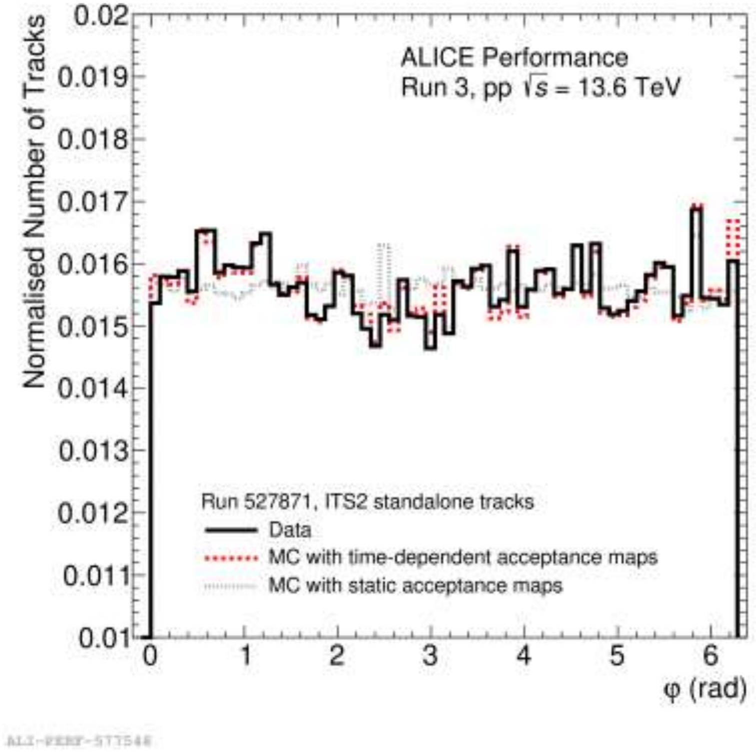
- Monitoring of cluster and track performance in offline reconstruction and Monte Carlo (MC) simulation

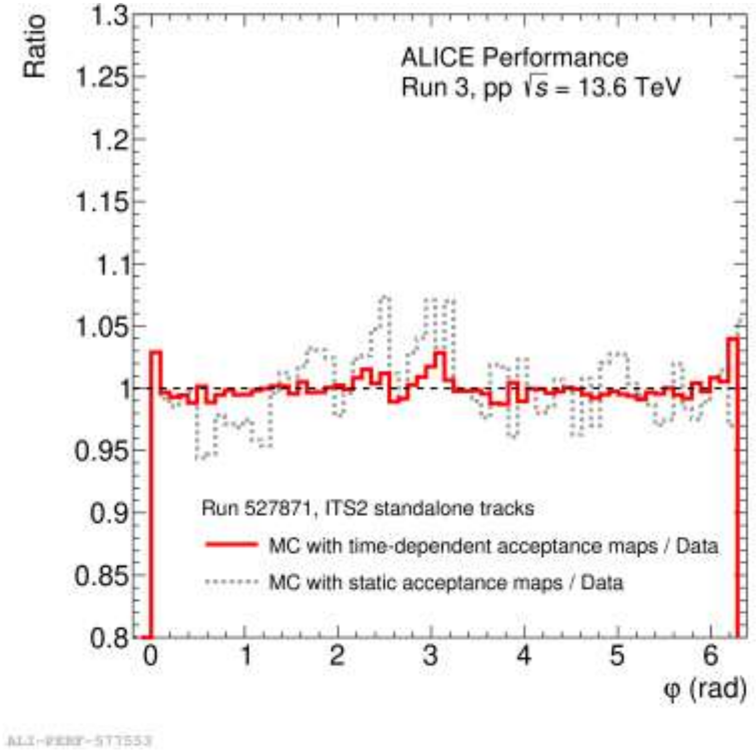


A Master thesis on QC from ***CCNU***

Time-dependent acceptance maps

- Various factors can lead to the loss of ITS2 high-speed links during data taking
- The DCS (detector control system) in-run recovery process typically requires approximately 10 s to restore them
- These inefficiencies are reflected in the cluster and track distributions
- A dedicated online calibration workflow has been implemented to monitor inefficient chips → enabling the generation of time-dependent acceptance maps → reproducible in Monte Carlo simulation

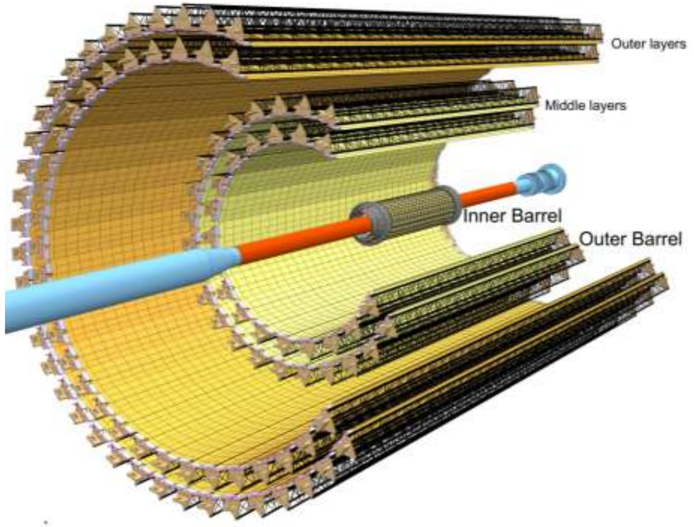


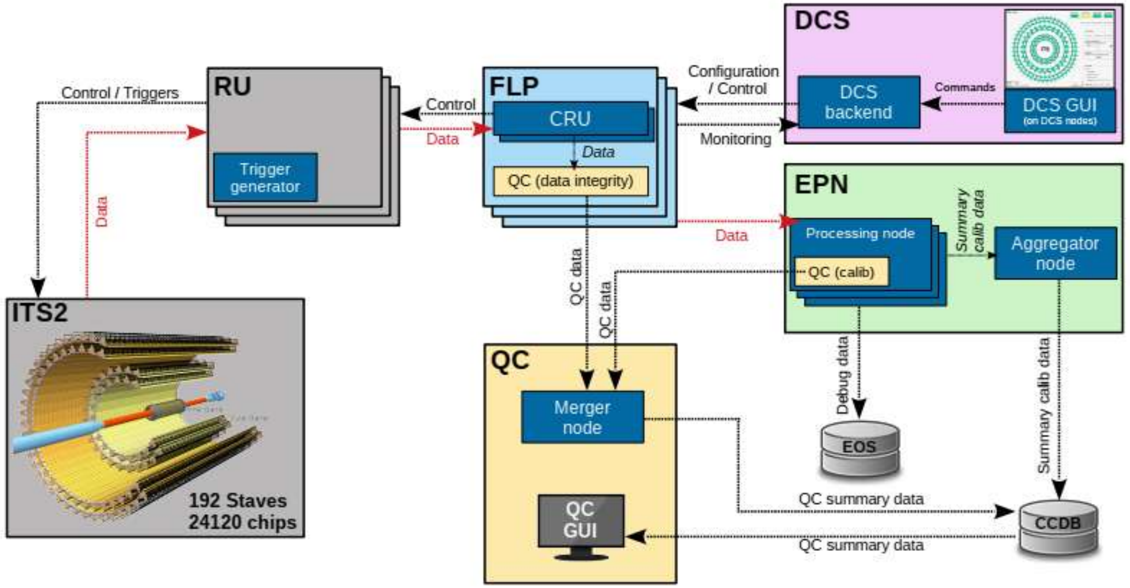


Calibration overview

- Main ITS2 calibrations
  - Threshold tuning
  - Noisy pixel masking

Challenging procedure:
- 24120 chips with 524288 pixels each → 12.5 Giga pixels → ~ 60 TB of event data (Full threshold scan)
- Online calibration workflows runs between LHC fills

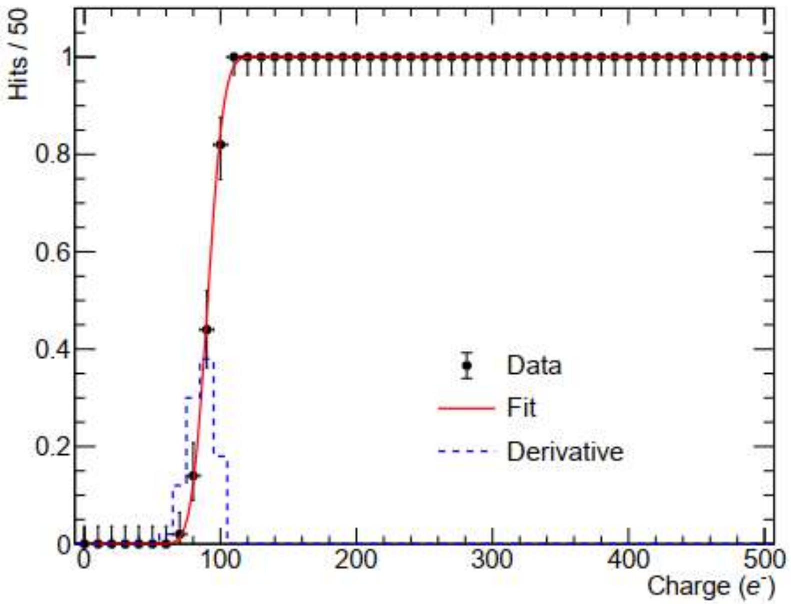


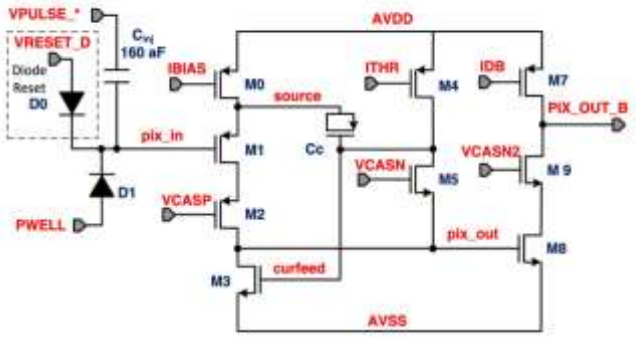


Scan	Objective	Frequency	Description
Short Threshold scan	Monitoring	~1/day	Measurement and monitoring of pixel thresholds
Threshold scan full	Monitoring	1/year	Measurement of thresholds used as reference
Digital/Analog scan	Calibration	<1/year	Tagging of problematic pixels and pixel columns
VCASN scan	Calibration	<1/year	Coarse tuning of pixel thresholds
ITHR scan	Calibration	<1/year	Fine tuning of pixel thresholds
VRESETD scan	Monitoring	1/year	Monitoring of VRESETD working point
Pulse shape scan	Monitoring	<1/year	Probing of the pixel analog signal shape
Noise scan	Calibration	~1/year	Detection of noisy pixels

Threshold (1/4)

- General threshold calibration operations
  - Inject charge into single pixels
  - Vary scan parameter and repeat
  - Measure response (hits per injection) as a function of the scan parameter
  - Fit response vs scan parameter with error function to extract 50%-point (threshold) and σ (noise)





Threshold scan

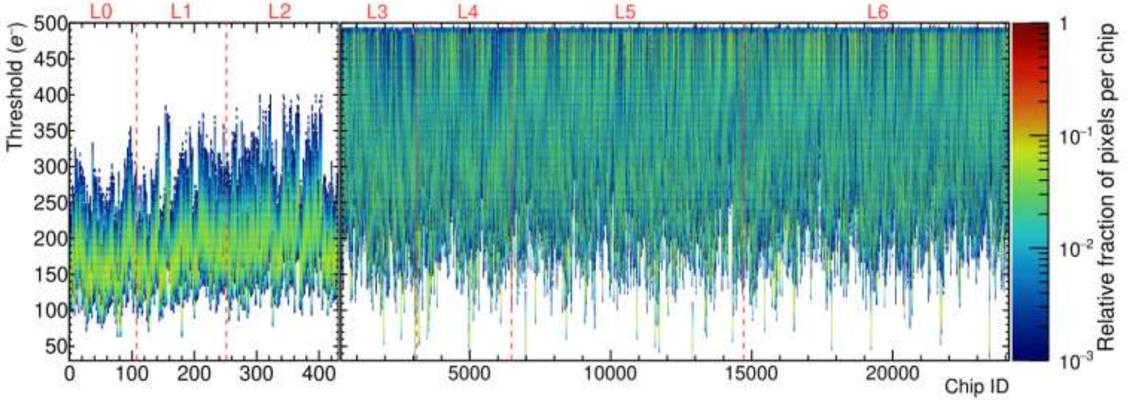
- Goal: measure the average threshold per chip
- Vary the charge injected keeping fixed the DACs setting
- Pixel threshold = inflection point of S-curve
- Chip threshold = mean of pixel thresholds
- Data stored for monitoring of detector stability over time
- ~2% of representative pixels per chip are scanned (daily threshold verification)

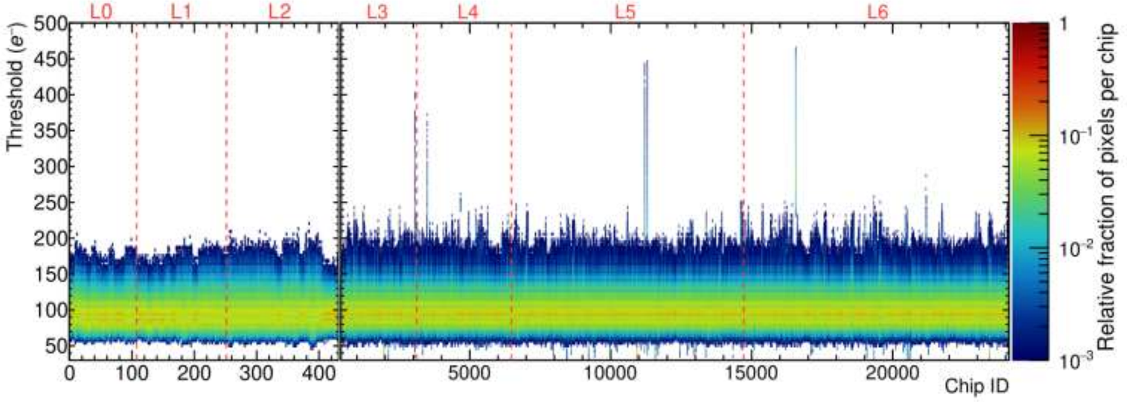
Threshold tuning

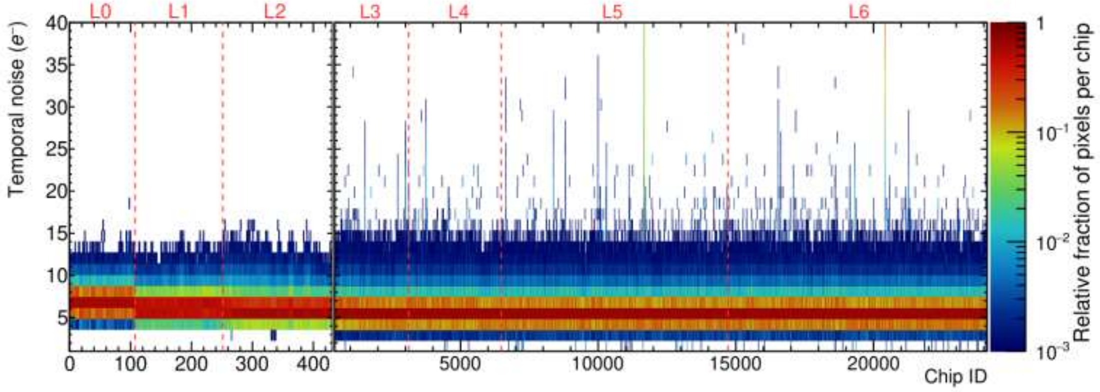
- Goal: set the operation point of the detector
- Threshold influenced by the setting of 2 DACs: VCASN and ITHR
- 2 different scans (chip level)
  - Inject a fixed charge varying the DAC settings
  - Fixed charge corresponding to desired threshold (~100 e-)
  - Tuned DAC values = inflection point of S-curve
- ~1% of representative pixels per chip are scanned

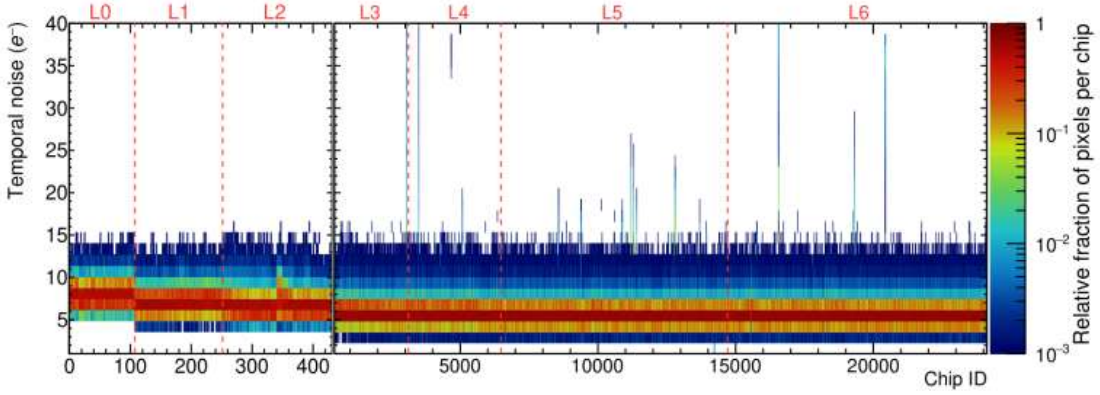
DAC: digital-to-analog converter

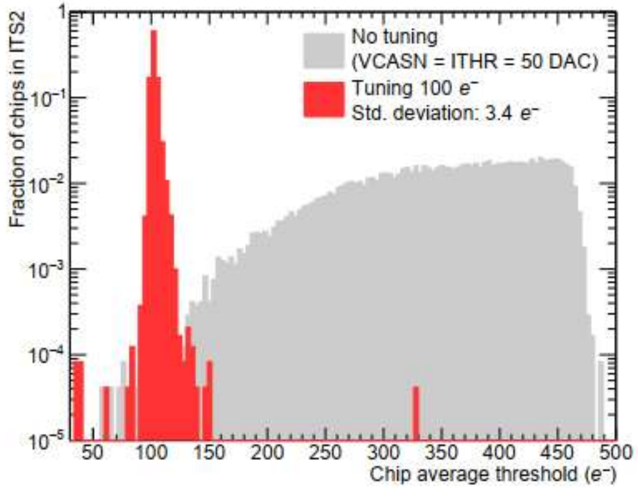
Threshold (2/4)





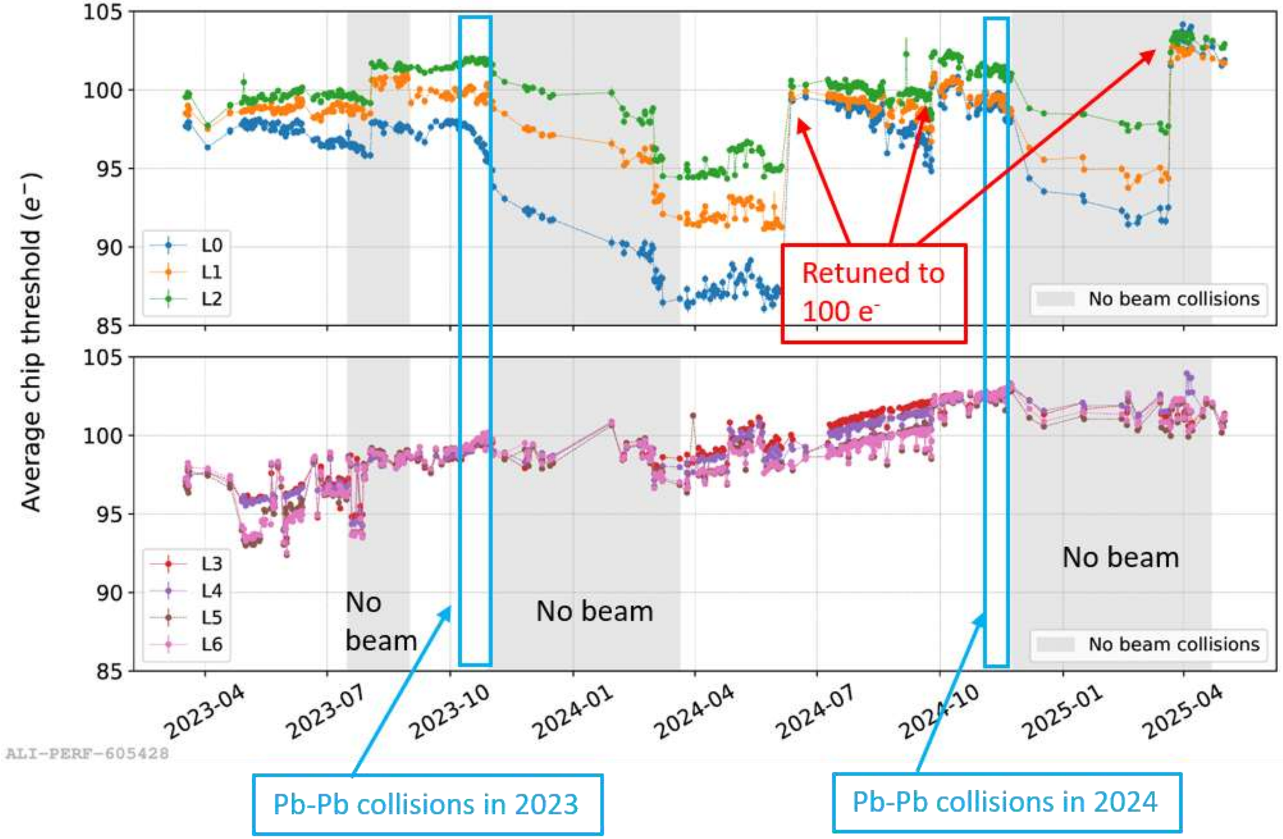


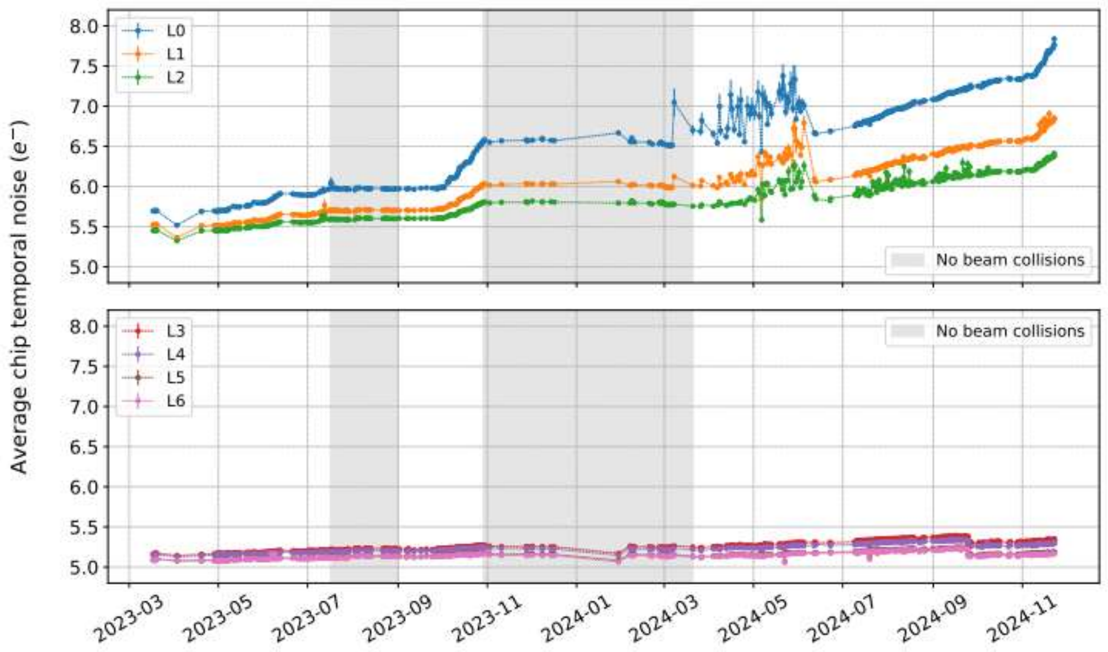




- Uniform response across the detector achieved (100 e^- target)
- Noise ~5 e^- (compatible with production QA measurements)

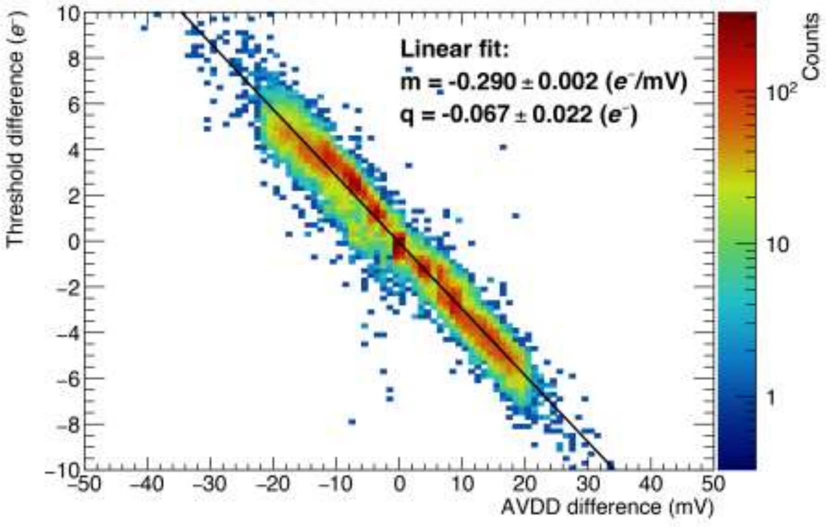
Threshold (3/4)

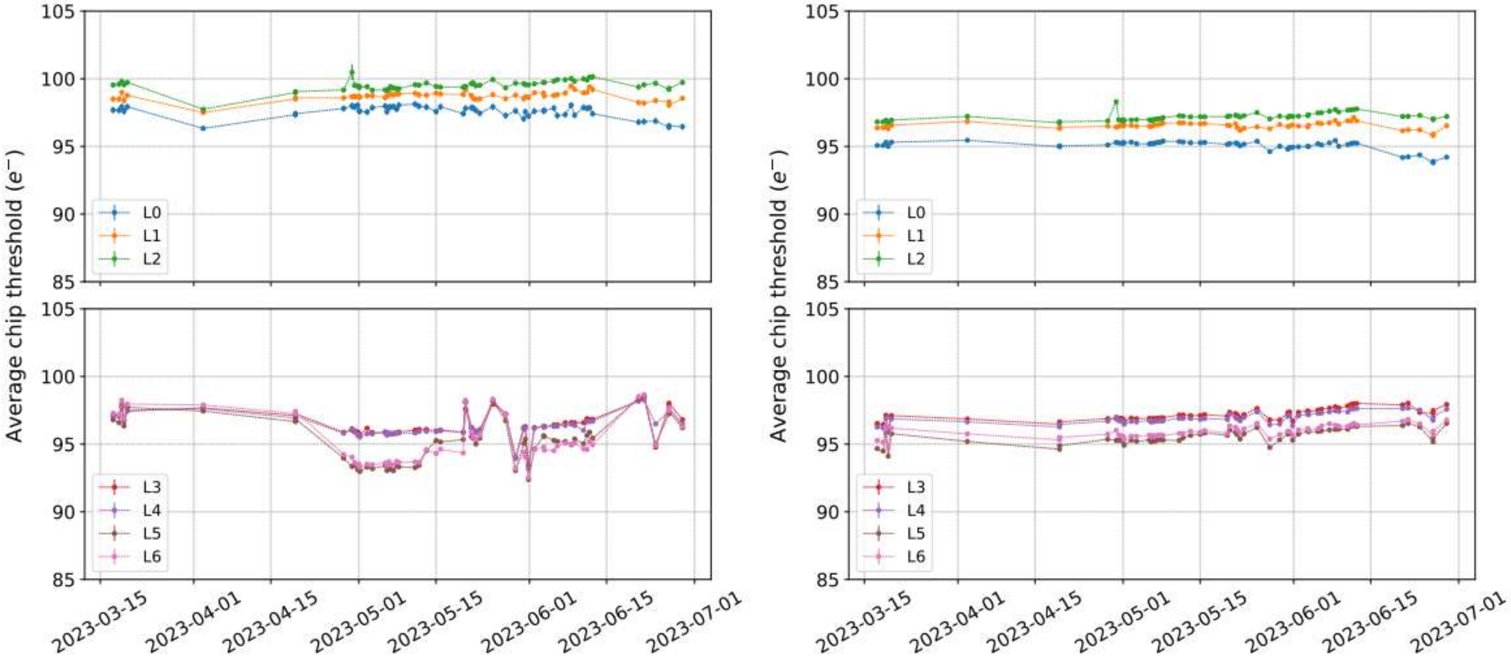




- Threshold stability has been consistently maintained across 24 k chips
  - Minor fluctuations due to supply voltage optimizations
- Increased noise over time (with radiation)
- Radiation effect observed in IB after Pb-Pb runs in 2023 and 2024
  - Effect compensated with new tunings in 2024 and 2025

Threshold (4/4)





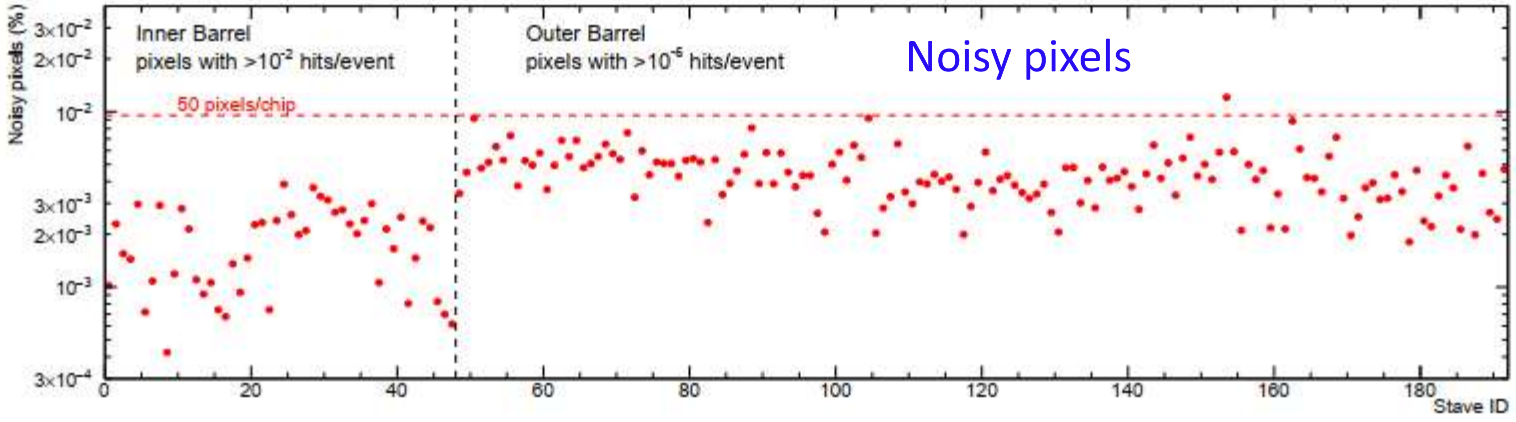
- Correlation between the threshold difference per HIC between a set of consecutive runs as a function of the AVDD difference per HIC for the same runs

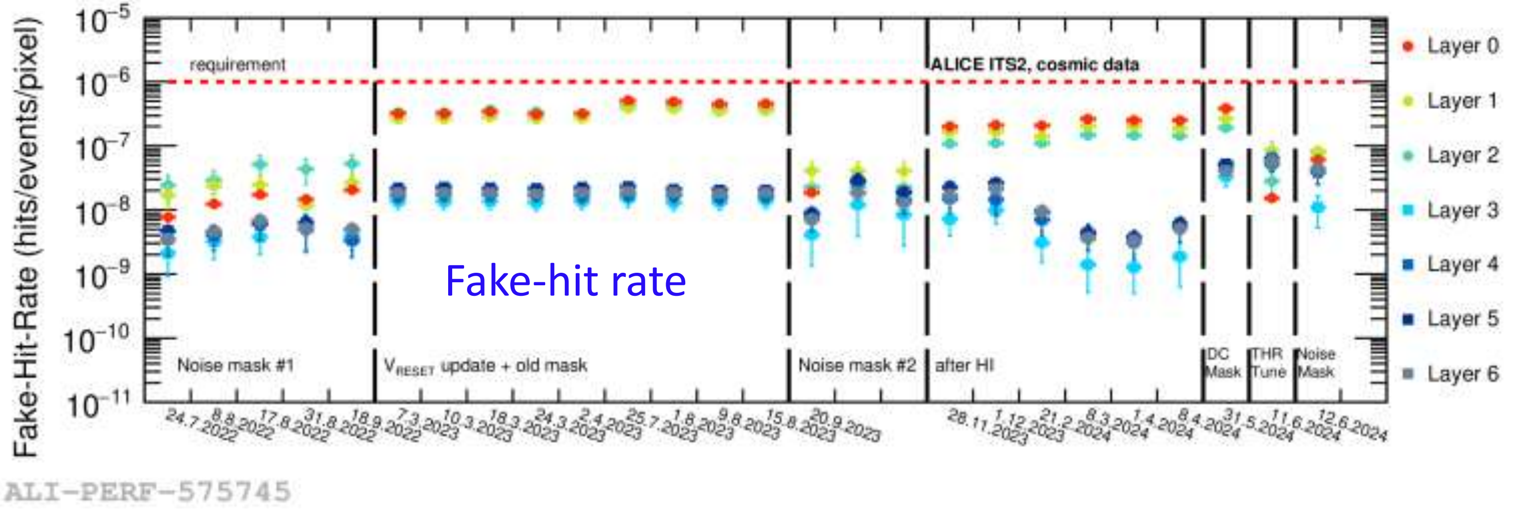
- Threshold trend from March to July 2023 without (left) and with (right) correction

Noisy pixel

- Possibility to run with static masks already proven during surface commissioning
- OB masking: pixels with 10^{-6} hits/event
- IB masking: 10^{-2} hits/event
  → almost no masking
  → prioritization of efficiency over data rate reduction
- Fraction of masked pixels: 0.004%
- Stable noisy pixel map → occasionally noise calibration is sufficient

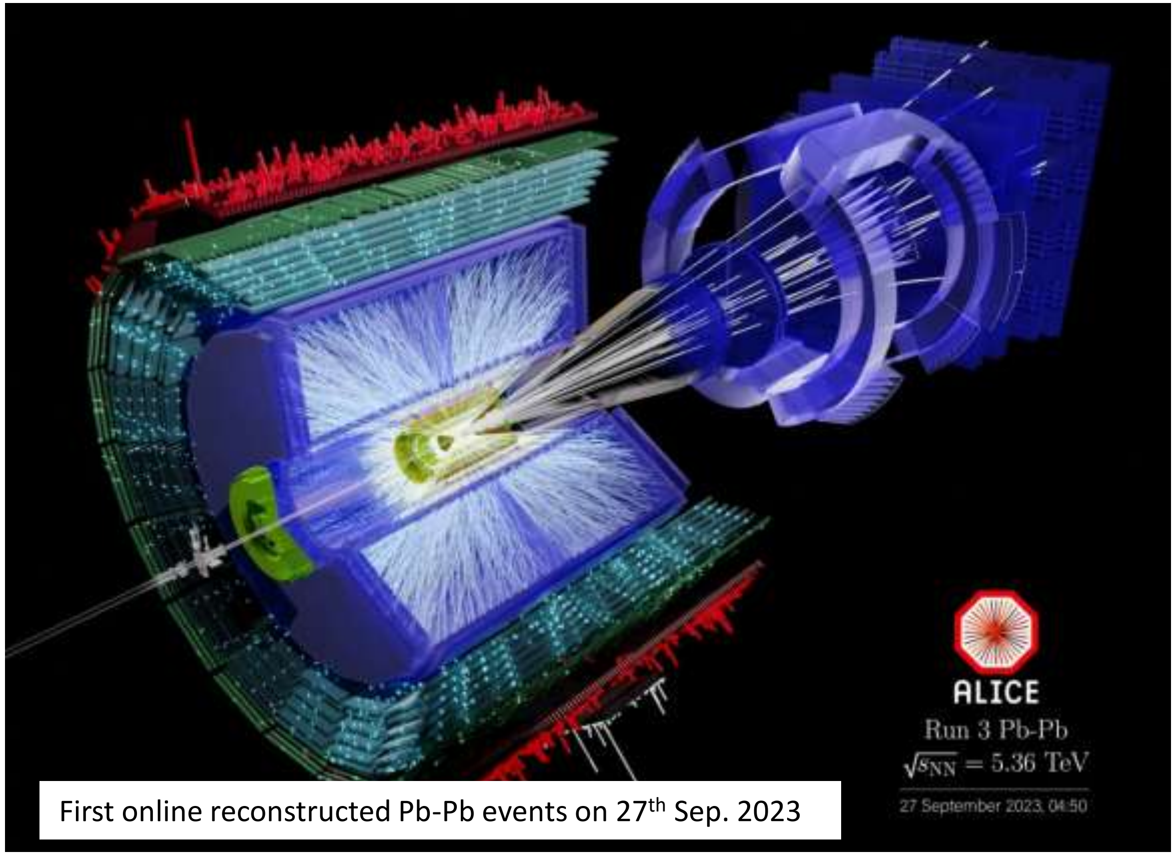
Extremely quiet detector!



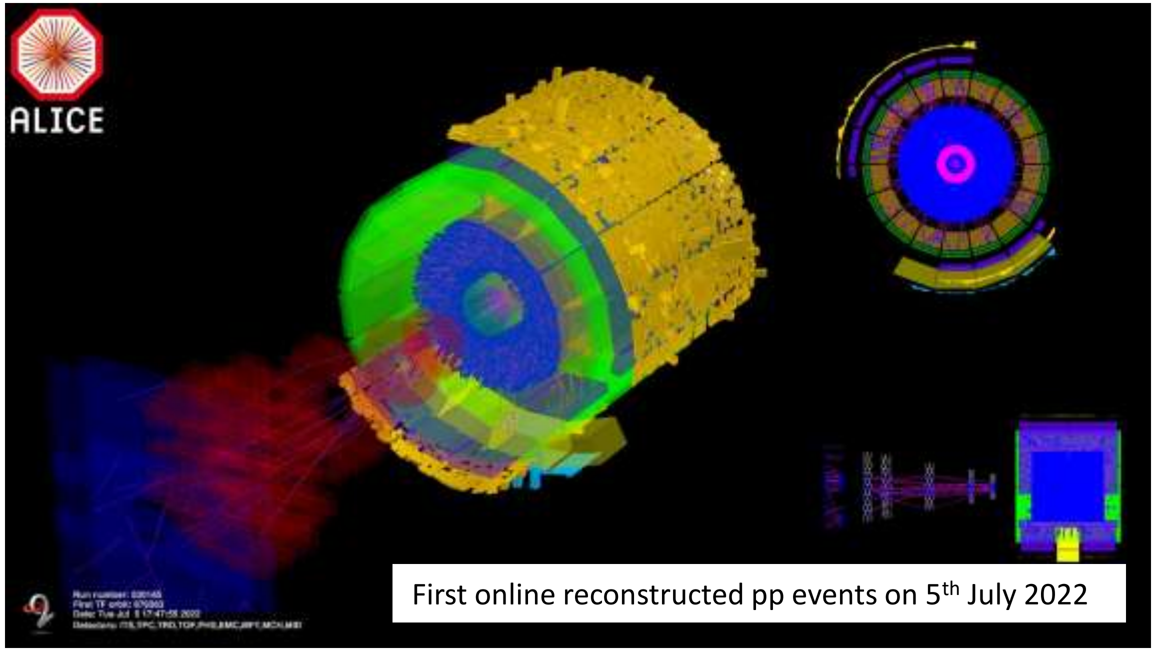


ITS2 in Run 3

- Integrated luminosity so far
  - pp collisions: ~127 pb^{-1}
  - Pb-Pb collisions: ~3.8 nb^{-1}
    - Recorded Minimum Bias sample of ~24 billion collisions, ~80 times larger than Run 1 and Run 2
- ALICE standard interaction rate
  - pp collisions: 500 kHz
  - Pb-Pb collisions: 50 kHz (achieved in 2024)
  - Instantaneous luminosity: ~10^{31} (pp) – 10^{27} (Pb-Pb) $cm^{-2}s^{-1}$



First online reconstructed Pb-Pb events on 27th Sep. 2023

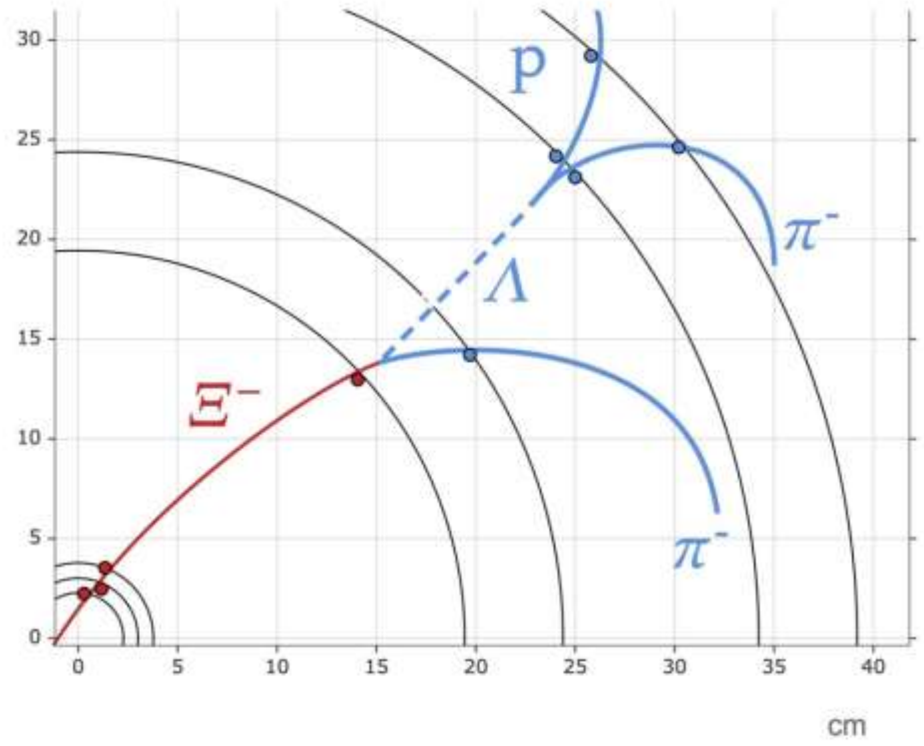


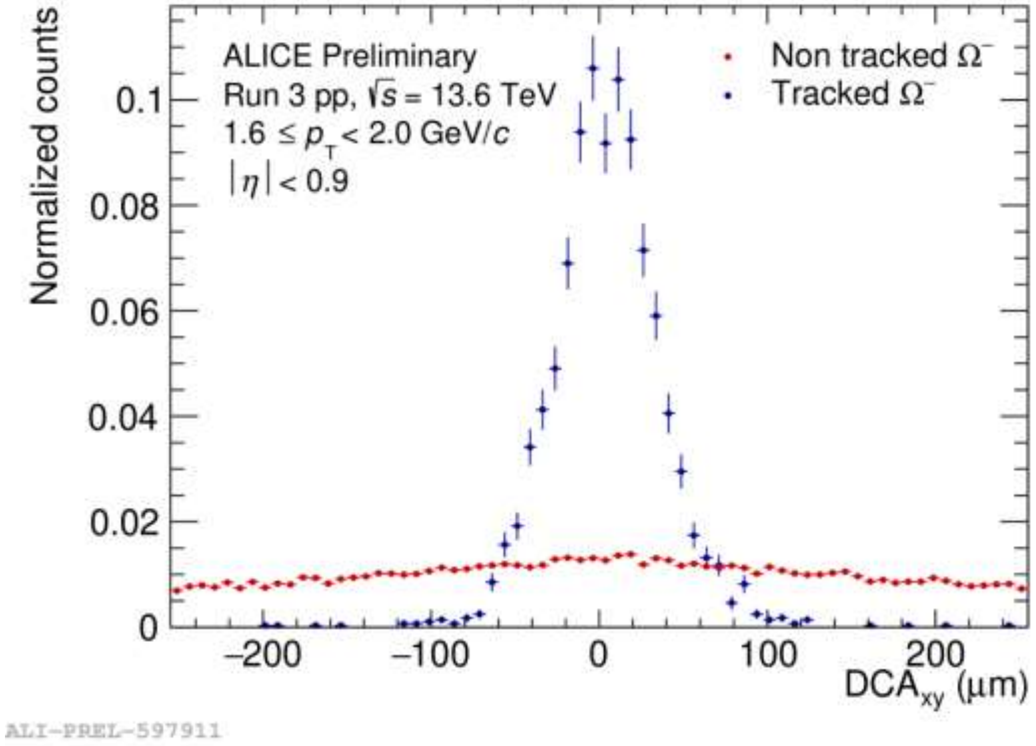
First online reconstructed pp events on 5th July 2022

- ITS2 demonstrated successful performance at visible interaction rates of up to 4 MHz in pp collisions
  - 3.5 MHz (visible) corresponds to 50 kHz Pb-Pb
- 99.6% pixel active in the whole detector
  - 94 chips broken/excluded, 970 k dead pixels and 500 k noisy pixels
- Loss of acceptance during run auto-recovered by DCS
- Sporadic data corruption events not affecting overall performance
  - Dominated by SEU induced issues; further consolidations ongoing

Detection of weakly decaying particles

- ITS2 Inner Barrel has the first three layers within 4 cm
  - Direct tracking of charged weak-decaying particles before their decay via strangeness tracking
  - New possibilities of studies: non-prompt cascades, hypernuclei, exotic bound states



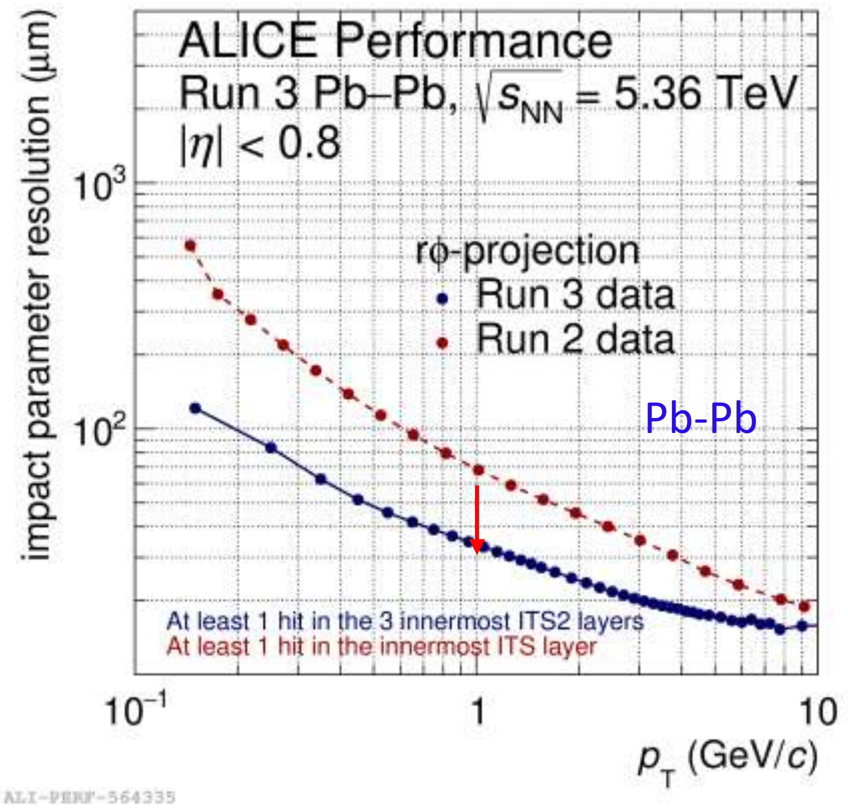


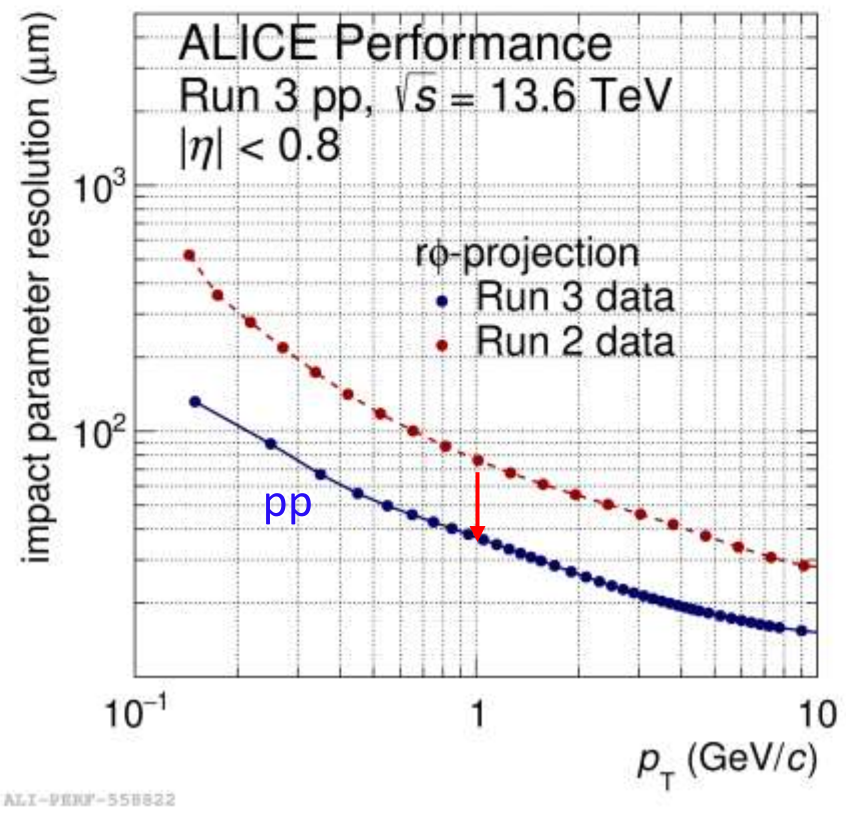
Impact parameter resolution of tracked Ω^- baryons: an order-of-magnitude improvement!

Impact parameter resolution

- ITS2 TDR
  - Factor 3 improvement wrt ITS1
- Measurement in Run 3
  - ~2x improvement at p_T = 1 GeV/c

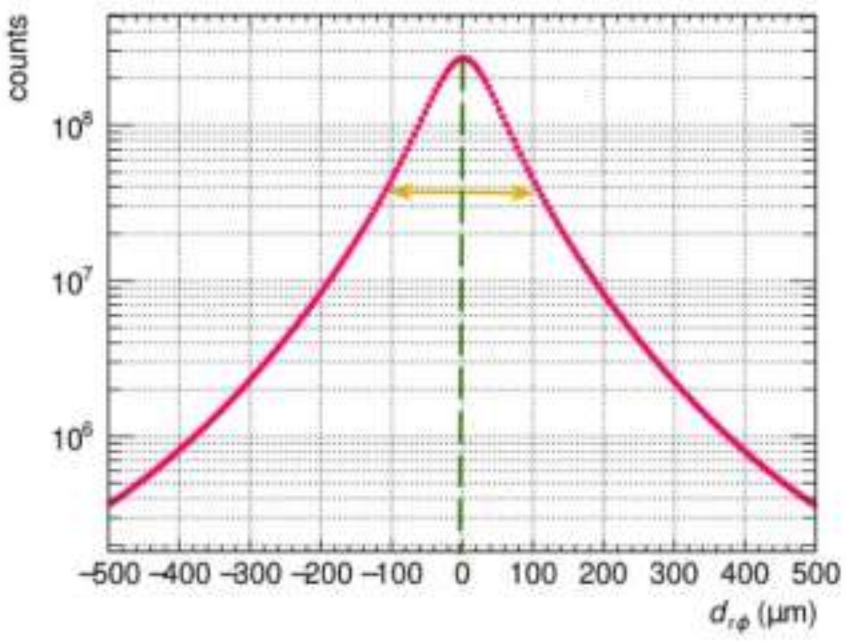
- Current simulations predict a factor 2.5 improvement over ITS1
  - Partially due to increase material budget ➡ 0.36% instead 0.3% X_0 per layer
  - Too simplified material description in the simulations

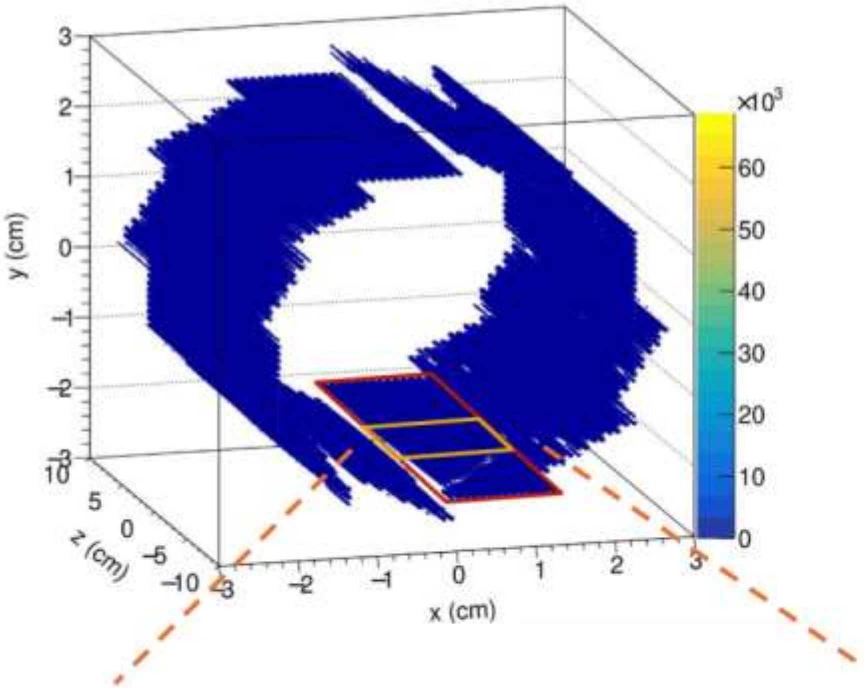


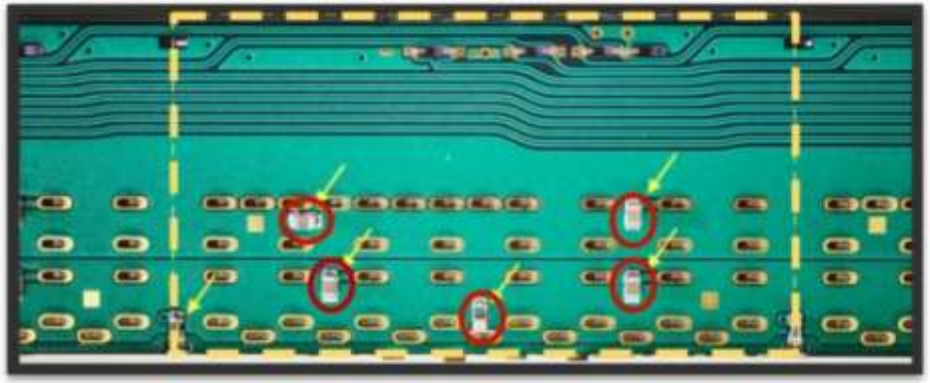


Impact parameter dependence on material (1/2)

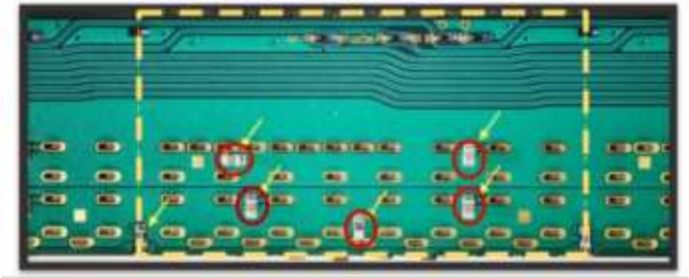
- Taking one stave on L0 (2.2 cm from the interaction point) to study the effects on material
  - Tracks are required to have good ITS+TPC quality and at least one hit on Layer 0



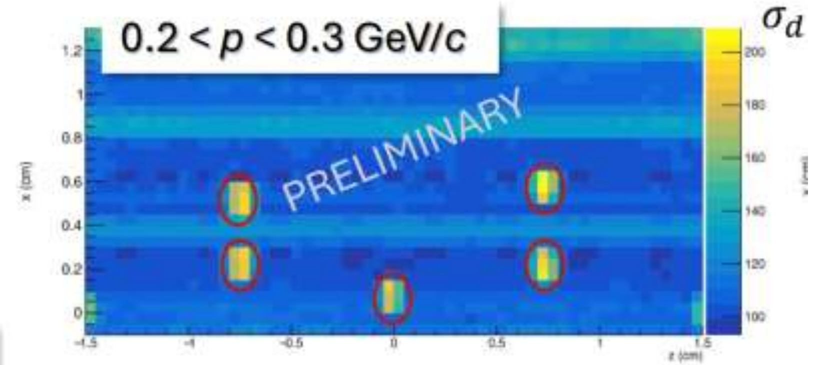


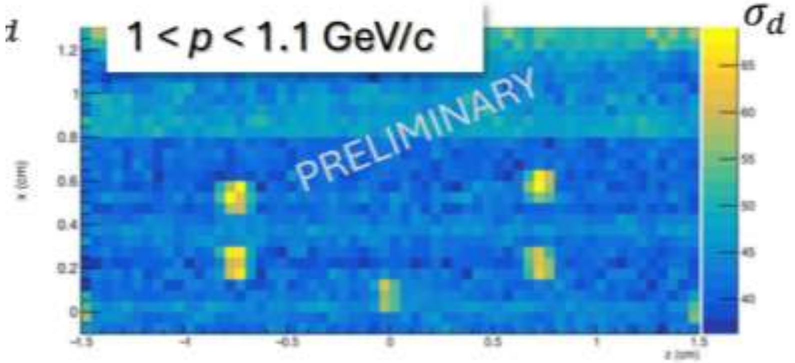


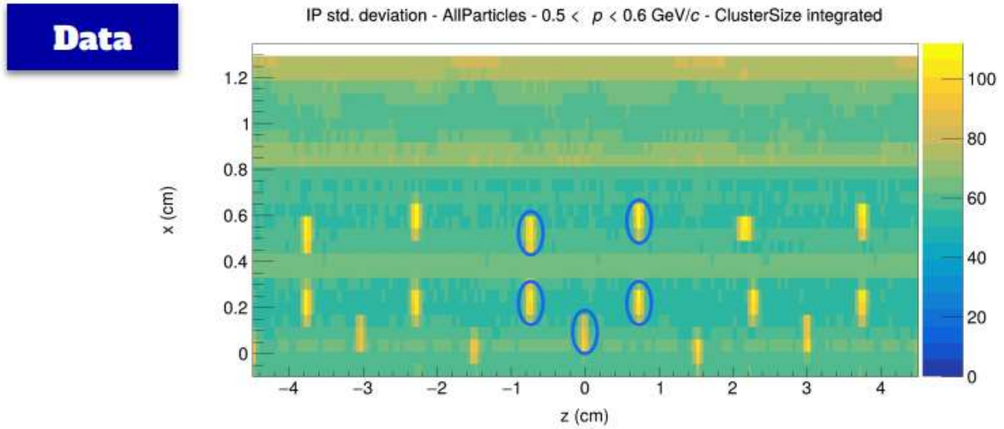
Impact parameter dependence on material (2/2)

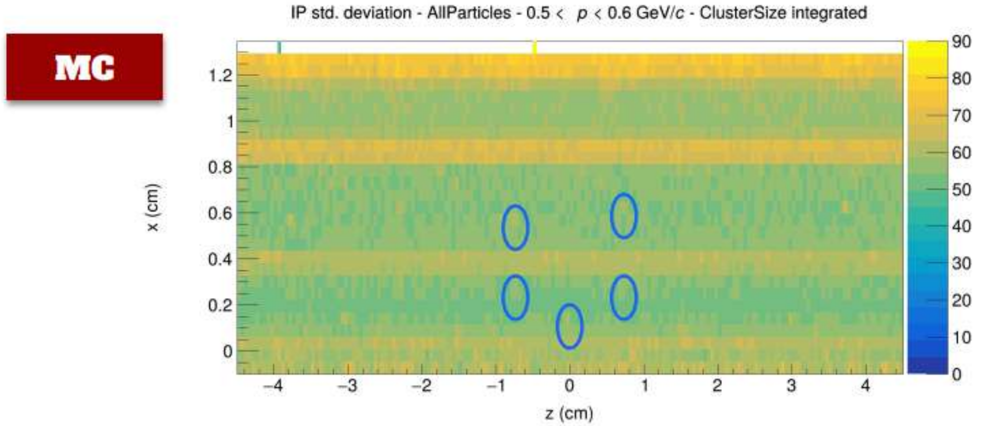


- A localized broadening of the distribution is observed near the capacitors (1×0.5 mm²)
- The effect diminishes with increasing particle momentum
- The capacitor material budget is not properly reproduced in the MC simulation



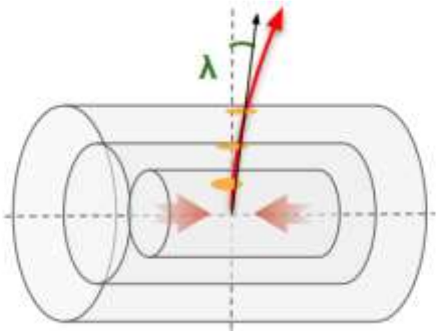


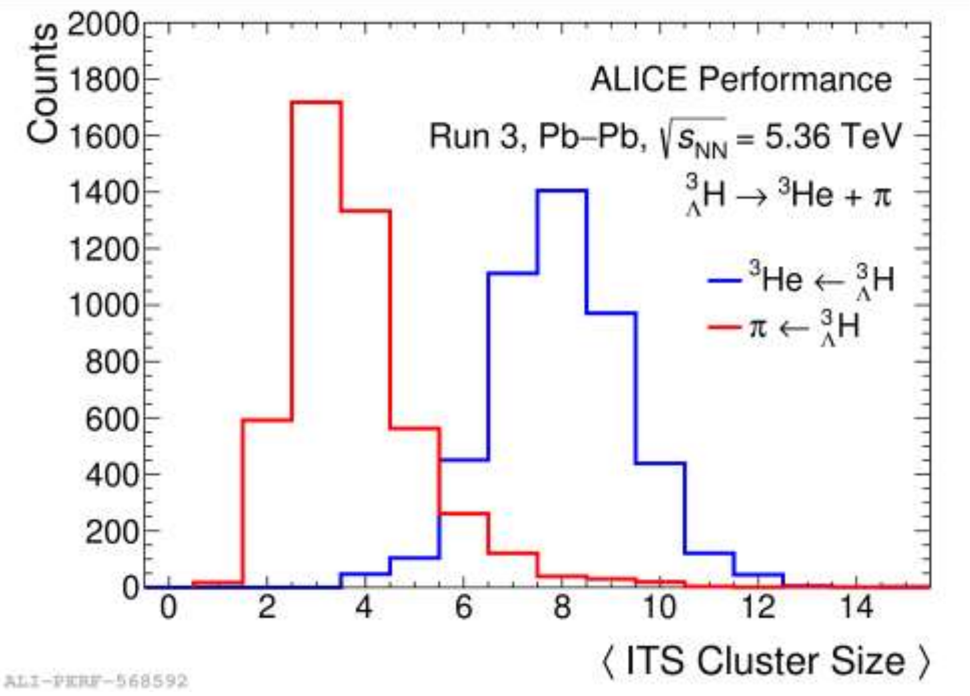


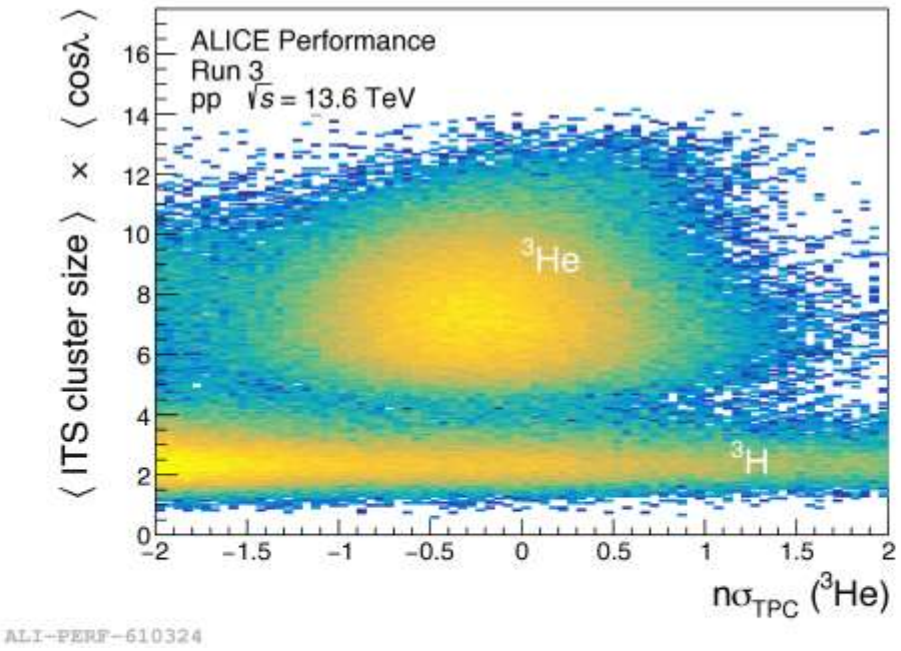


Cluster-size-based PID

Cluster size depending on track inclination λ and specific energy loss dE/dx







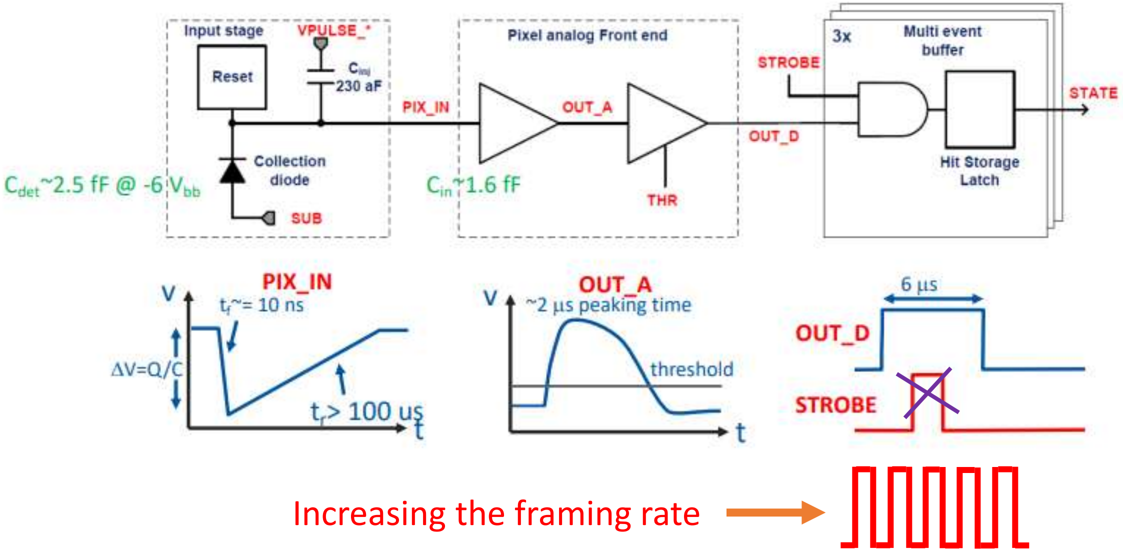
Hypernuclei in Pb-Pb

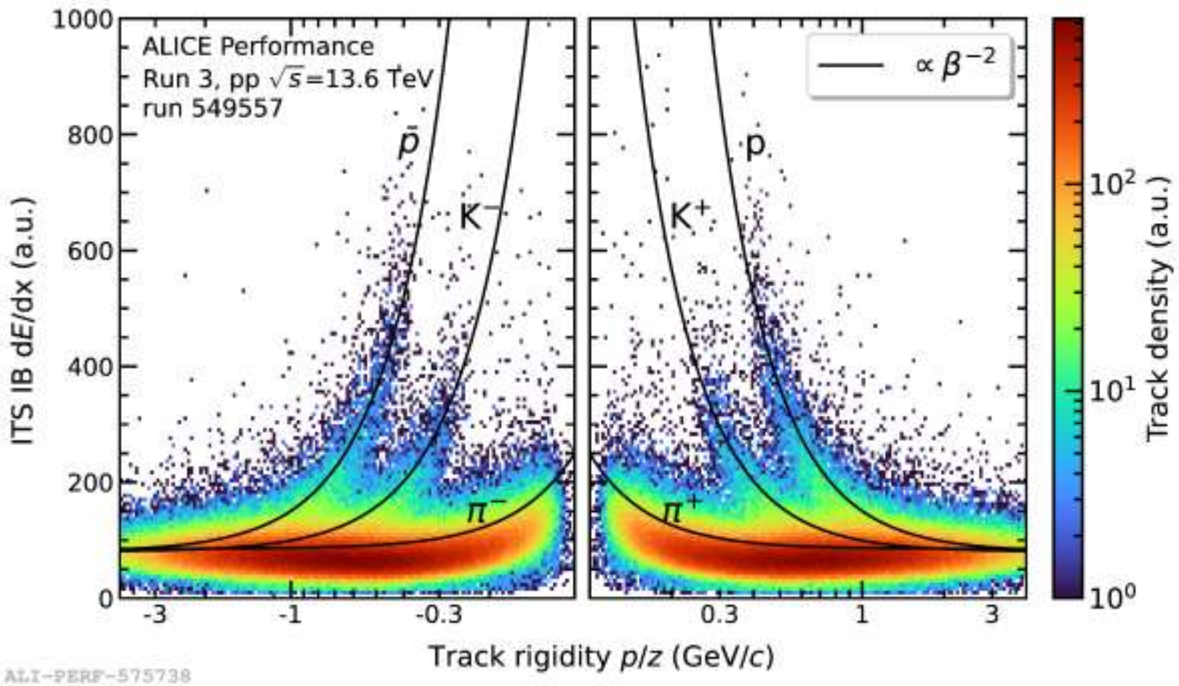
- Use of ITS2 cluster size to tag ^{3}He daughter track from hypertriton decay and reduce ITS-TPC fake matchings

- Light nuclei in pp
  - ^{3}He is selected using the TPC
  - ITS cluster size can be used to suppress the ^{3}H background

Energy-loss-based PID (2/2)

- Proof of concept for PID with thin binary readout
  - Dedicated ITS2 runs in pp with interaction rate at ~1kHz
    - Front-end tuned for charge-proportional analogue pulse length
    - 2.2 MHz framing rate on IB → oversampling ALPIDE response
  - First dE/dx spectrum observed!
  - Confirmed the potential of performing energy-loss-based PID with thin active volume MAPS

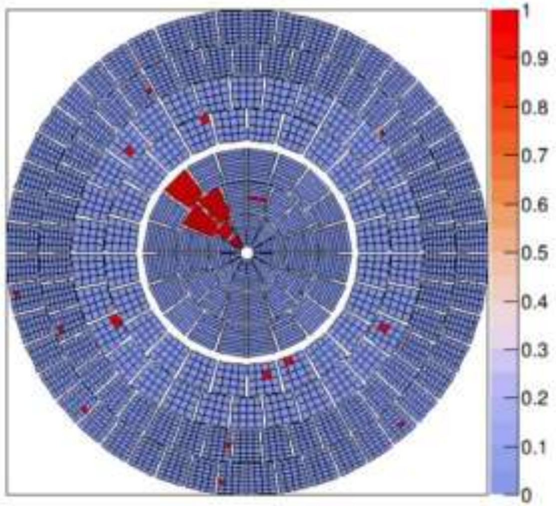




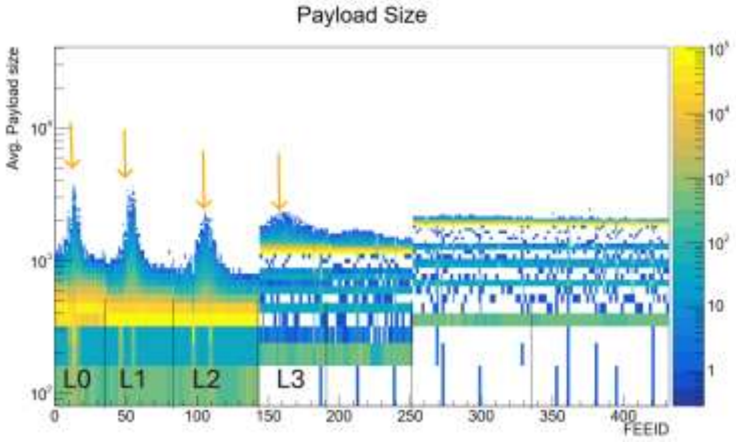
Lessons learned – beam background

In the first minutes of stable Pb-Pb beams in 2023, anomalies were observed in QC at $\varphi \simeq 2.4$, peaked at r = 2 to 4 cm

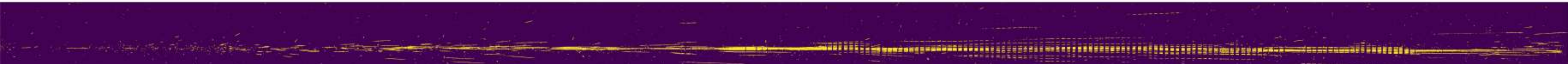
- Analysis of cluster shapes revealed MIP-like trajectories, originating roughly 100 meters away and traversing the detector at shallow angles
- The source was promptly identified and largely mitigated (refer to R. Bruce's report) → only first 10% of the statistics in 2023 affected
- Large clusters also observed in pp collisions at similar positions but with different properties
- Further investigations ongoing to understand the origin of the remaining background
- RU firmware was enhanced to manage these events more effectively



Inefficient map in Pb-Pb background



The ITS3 readout architecture enables full readout of such events by dropping the subsequent ones


Example hit-map on L0_04 in Pb-Pb collisions

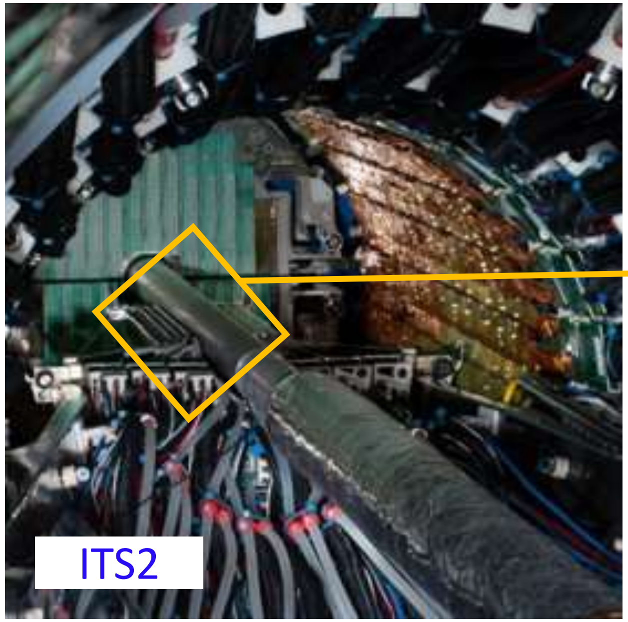

Example hit-map on L0_04 in pp collisions

~1.5 cm
(single chip)

IB stave: ~27 cm

ITS2 today and the road ahead

- ITS2
  - The first Monolithic Active Pixel Sensor based detector at LHC, was installed in ALICE during the LS2
  - Excellent performance observed in both pp and Pb-Pb collisions
- ITS3 (LS3, 2026-2030): replacement of inner barrel of ITS2 with stitched wafer-scale 65 nm CMOS sensors to reduce material budget and improve pointing resolution



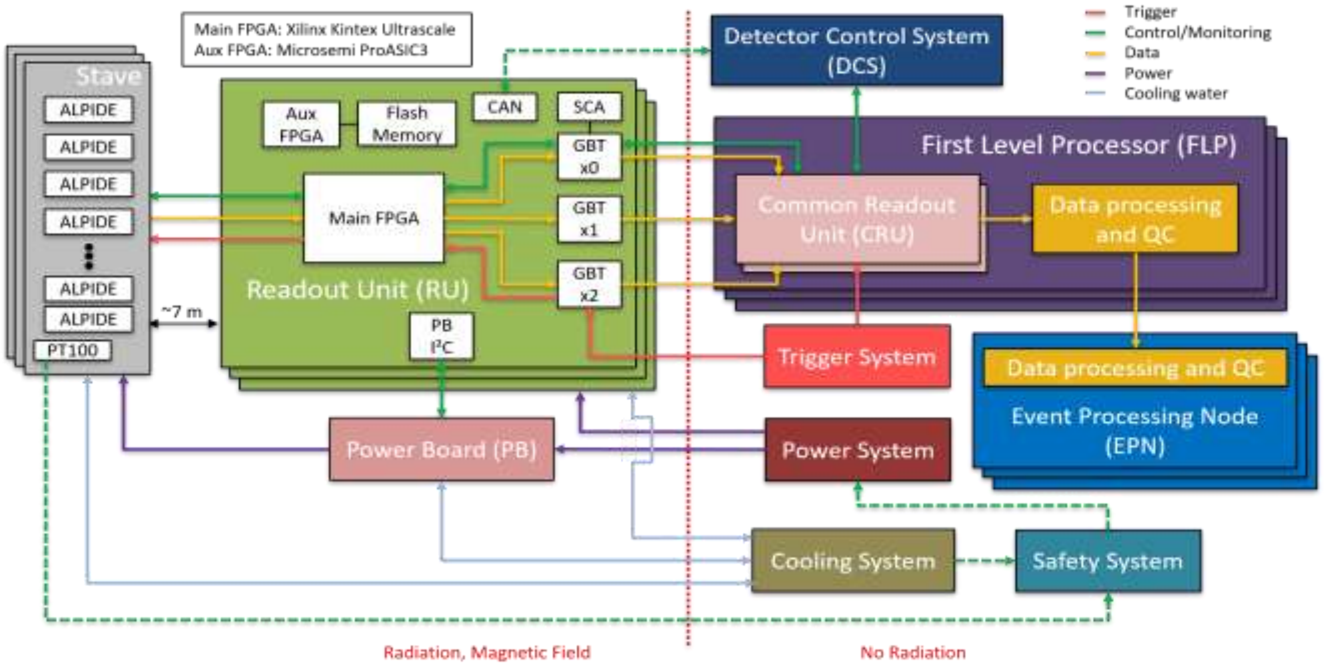
Backup

ITS1 vs ITS2

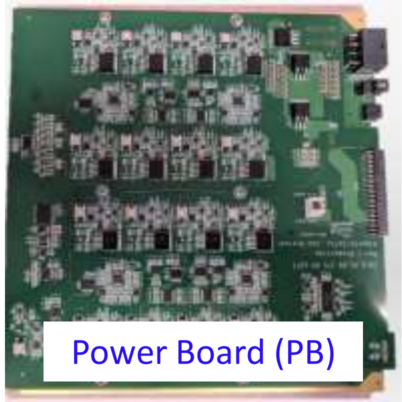
	ITS1	ITS2
Technology	Hybrid pixel (SPD), strip (SDD), drift (SSD)	MAPS
No. of layers	6	7
Radius	39–430 mm	22–395 mm
Rapidity coverage	$\lvert\eta\rvert \leq 0.9$	$\lvert\eta\rvert \leq 1.3$
Material budget / layer	SPD: 1.14% X_0	inner barrel: 0.36% X_0
	SDD (including thermal shield): 1.52% X_0	outer barrel: 1.10% X_0
	SSD (including thermal shield): 1.16% X_0	
Pixel size	SPD: 425 µm× 50 µm	27 µm × 29 µm
Spatial resolution ($r\varphi \times z$)	SPD: 12 µm × 100 µm	5 µm ×5 µm
Readout	Analogue (drift, strip), Digital (Pixel)	Digital
Max rate (Pb-Pb)	1 kHz	50 kHz

SPD: Silicon Pixel Detector
SDD: Silicon Drift Detector
SSD: Silicon Strip Detector

ITS2 system architecture



Readout Unit (RU)



Power Board (PB)

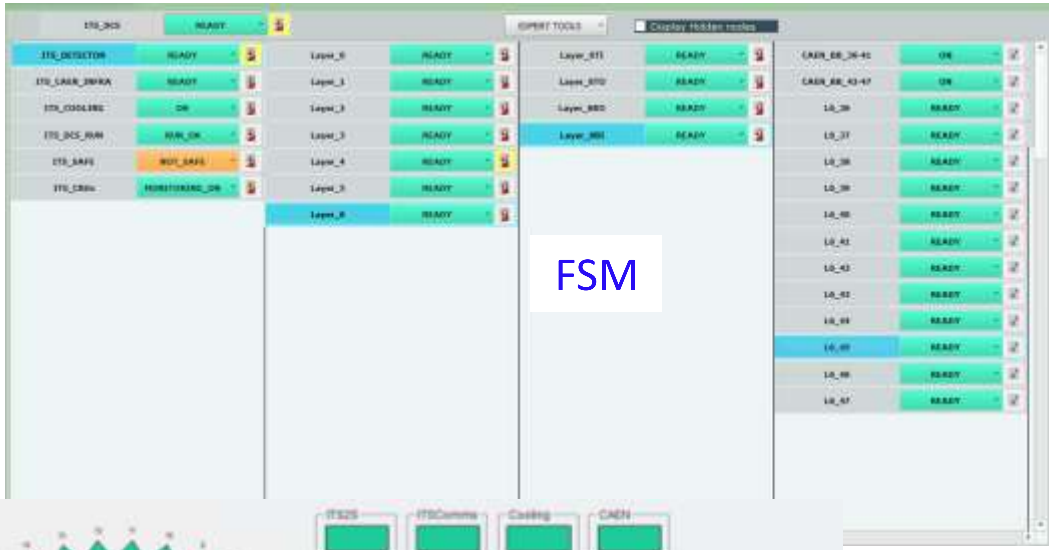
Common Readout Unit (CRU)

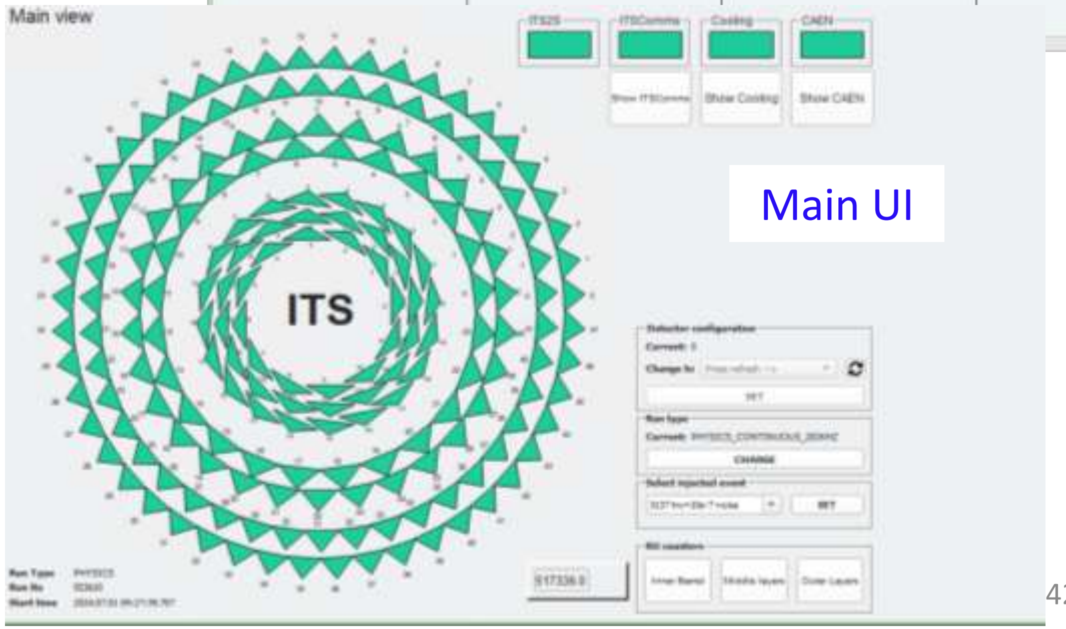
CAEN power system

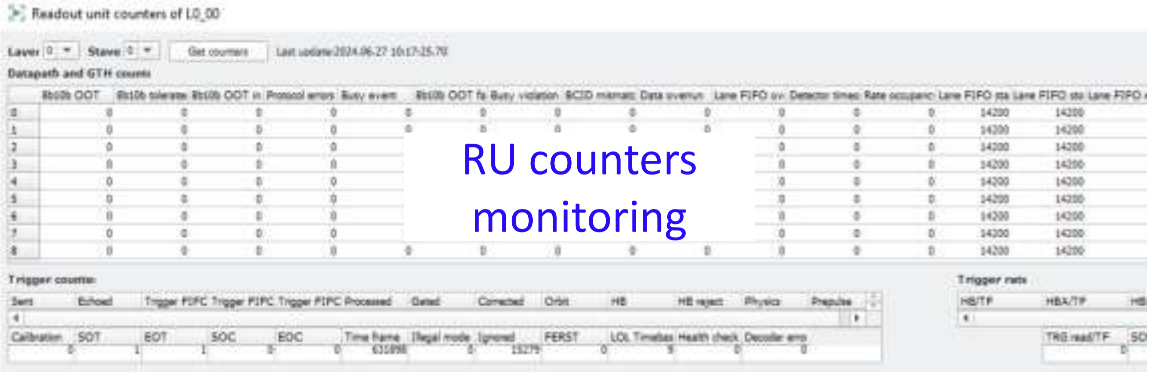
- Electrical links (~7 m) between the detector and the RU
- FPGA in radiation environment controlling detector, packaging data, electrical optical conversion using Versatile Link controlling powering
  - Needs scrubbing and TMR (Triple Modular Redundancy) to mitigate radiation effects
- Connecting to 22 CRUs hosting on 13 FLPs via the optical Versatile Link for raw data processing
- Detector Control System (DCS) communicates with the detector via CRU and RU
  - Automatic in-run recovery maximizes detector acceptance and data-taking efficiency
- Dedicated online/offline QC tasks to monitor data quality in data taking and calibration scans

DCS and safety system

- DCS
  - User interface (UI) developed in WINCC OA SCADA
  - Logics implemented as a Finite State Machine (FSM)
  - Detector operation and monitoring
    - Control the detector itself and its infrastructure, like RU/PB and cooling system
    - Monitoring > 100 k data points with data archiving
    - Automatic in-run recovery maximizes detector acceptance and data-taking efficiency
- ITS2S
  - Independent safety system
  - Interlocks CAEN power channels based on stave temperatures and cooling plant loop status

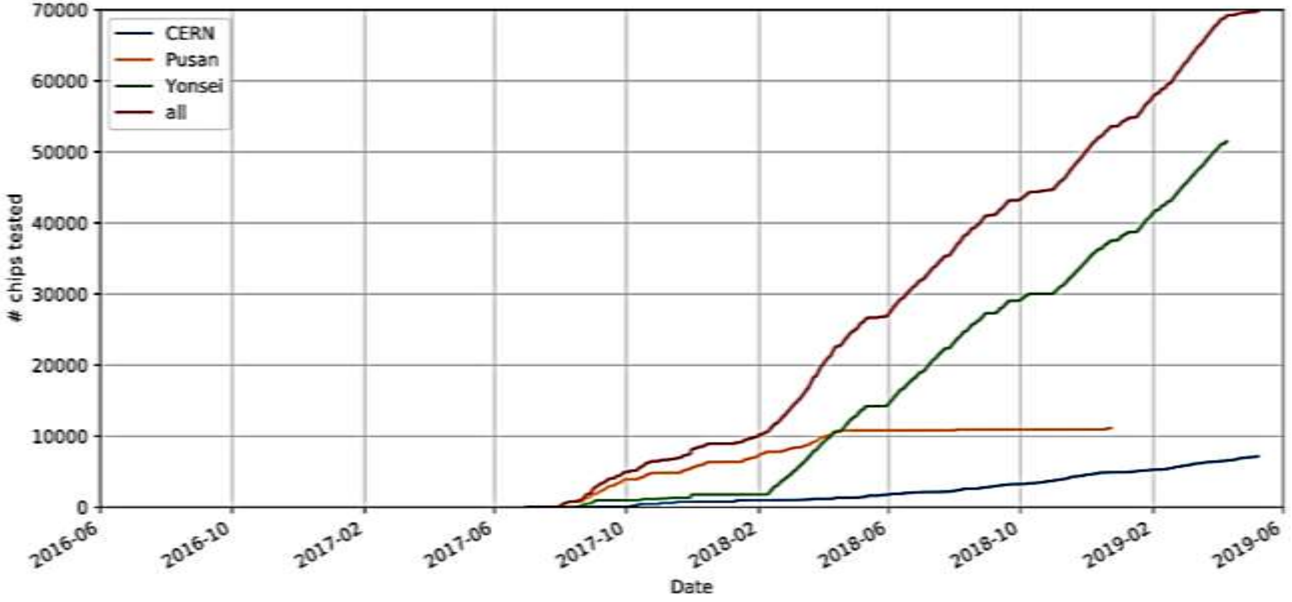




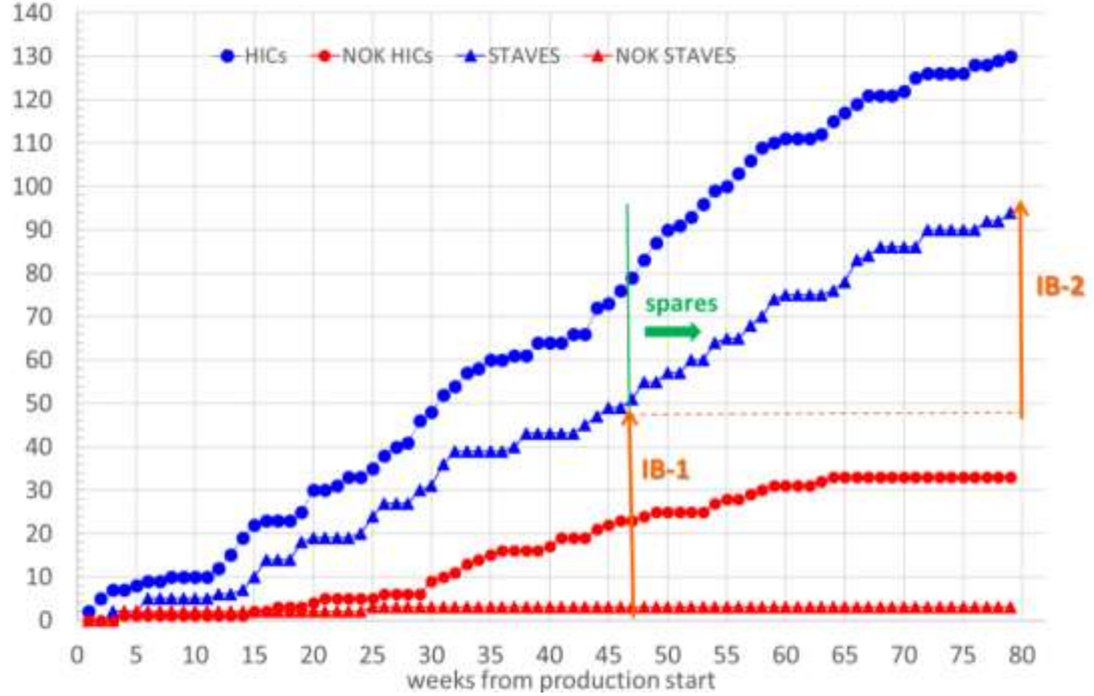


Sensor test, IB HIC/Stave production

Series test for the ALPIDE sensor



Inner barrel HIC & stave production



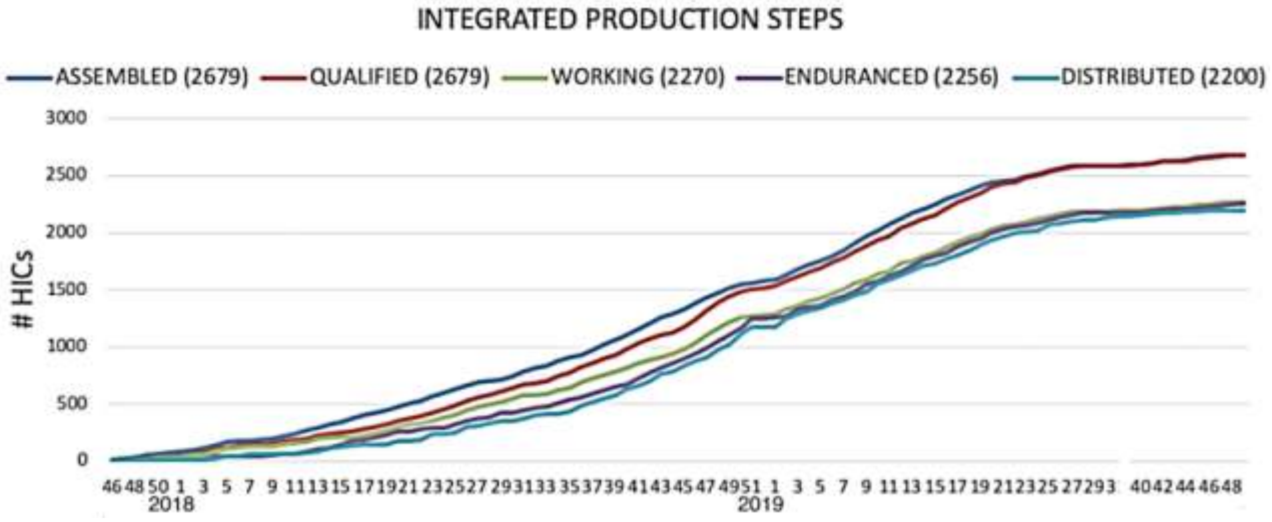
ALPIDE sensor test

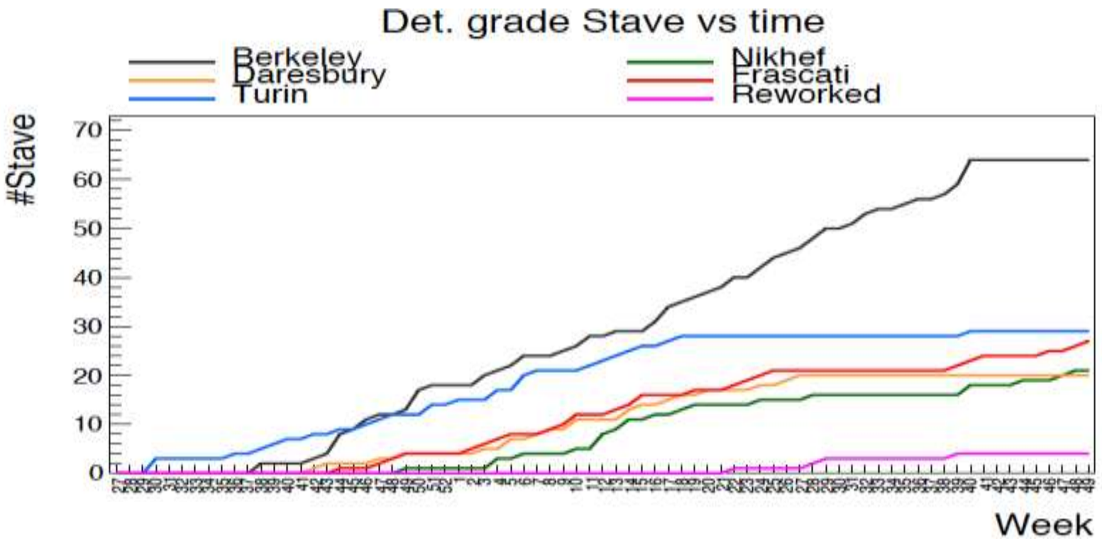
- Series test sites:
  - 50 µm sensors for IB: CERN
  - 100 µm sensors for OB: Pusan/Inha and Yonsei
- Total sensors tested: ~70000
- Completed in May 2019
- Yield: ~63.7%

IB HIC and stave production

- Production site: CERN
- 95 staves assembled, enough for two IB sets plus spares
- Completed in May 2019
- Yield: ~73%

OB HIC/Stave production





OB HIC production:

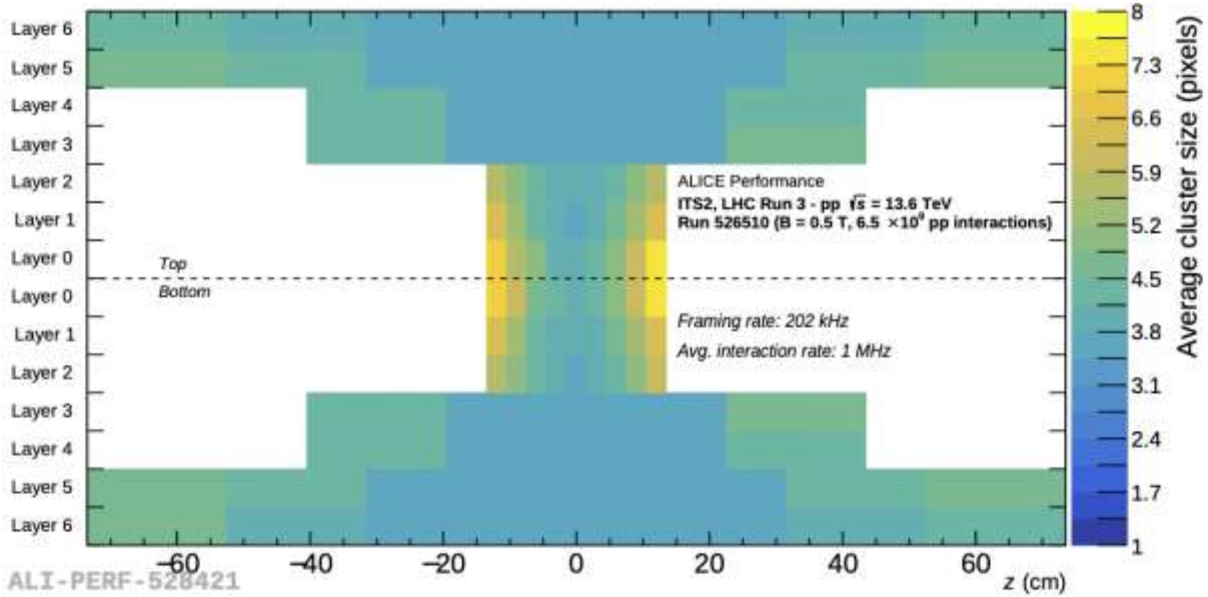
- HIC assembly sites: Bari, Liverpool, Pusan/Inha, Strasbourg and Wuhan
- FPC test and preparation sites: Catania and Trieste
- Production completed in November 2019
- 2679 HICs assembled and 2270 HICs qualified as Detector Grade (DG)
- 2200 HICs distributed to OB stave production sites
- Yield: ~84.7%

OB stave production:

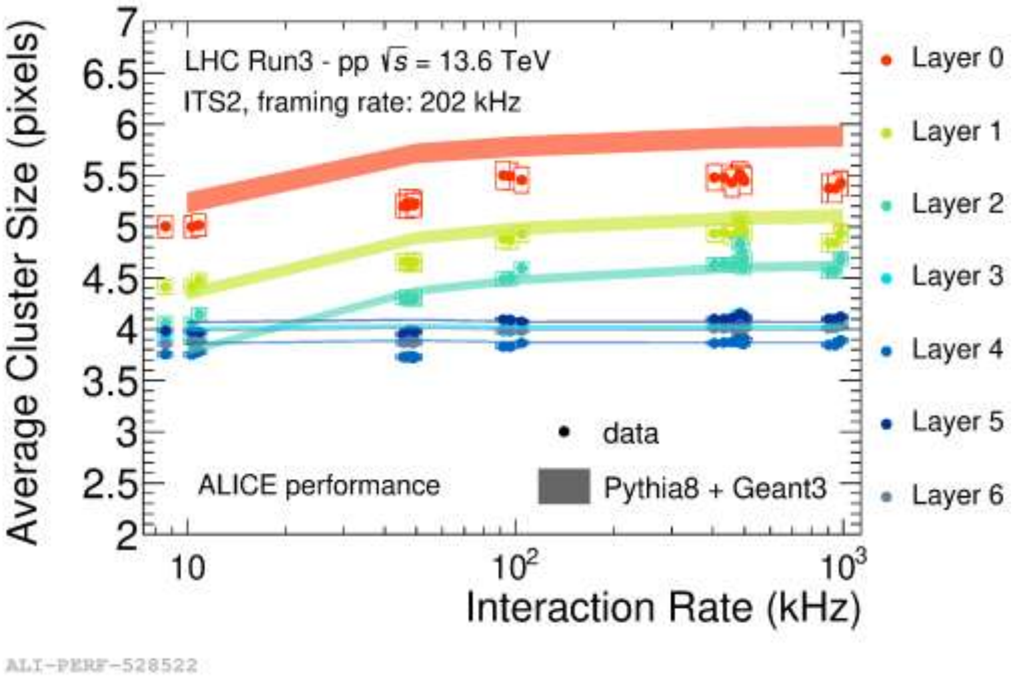
- Production sites: Daresbury, Frascati, Nikhef and Turin (for OL), Berkeley (for ML)
- 68 (64 DG) ML staves + 107 (101 DG, including 4 reworked) OL staves assembled
- ML production completed in Octber 2019
- OL production completed in December 2019
- ML yield: ~94%
- OL yield: ~94%

Cluster size

- Cluster size averaged for half layers (pp)
  - Between 3 and 8 pixels depending on η
  - RMS ranging on the same interval
  - Observed to be stable over time
  - Independent of the interaction rate

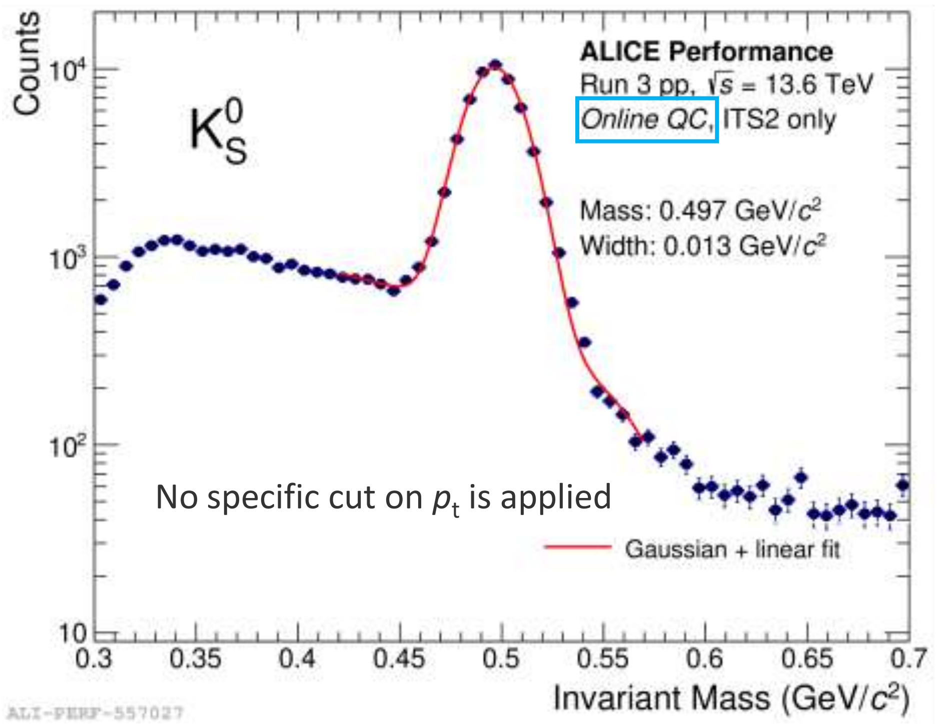


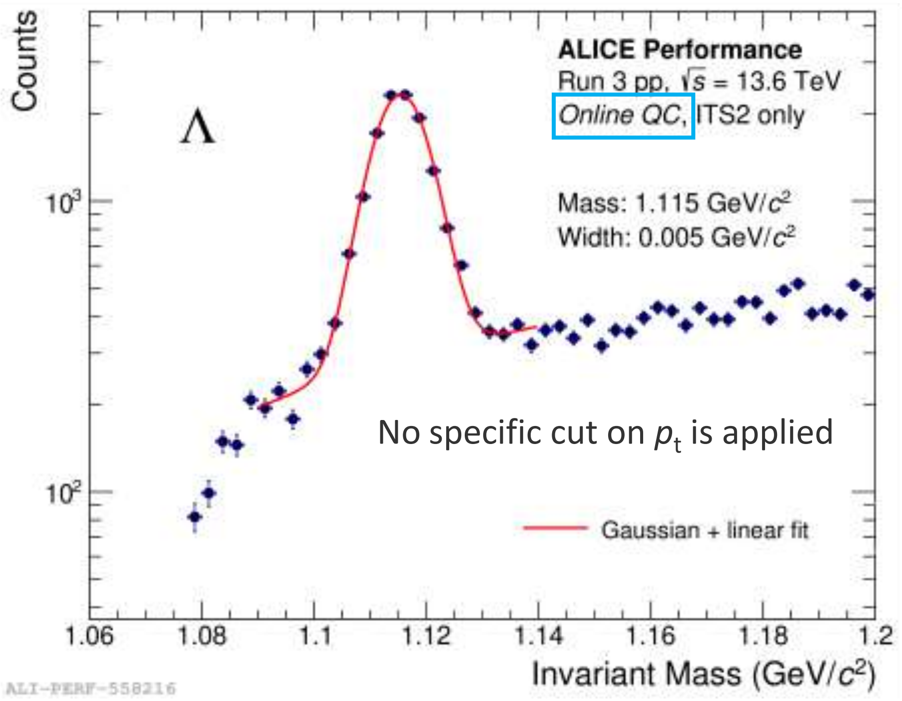
- Simulation with Pythia 8 + Geant 3 (pp)
  - Simulated noise: $2x10^{-8}$ hits/event/pix (IB), $3x10^{-9}$ hits/event/pix (OB)
  - Good agreement with data considering approximations
    - Average noise per barrel and not per stave/chip
    - Limited statistics in MC: ~20 k events



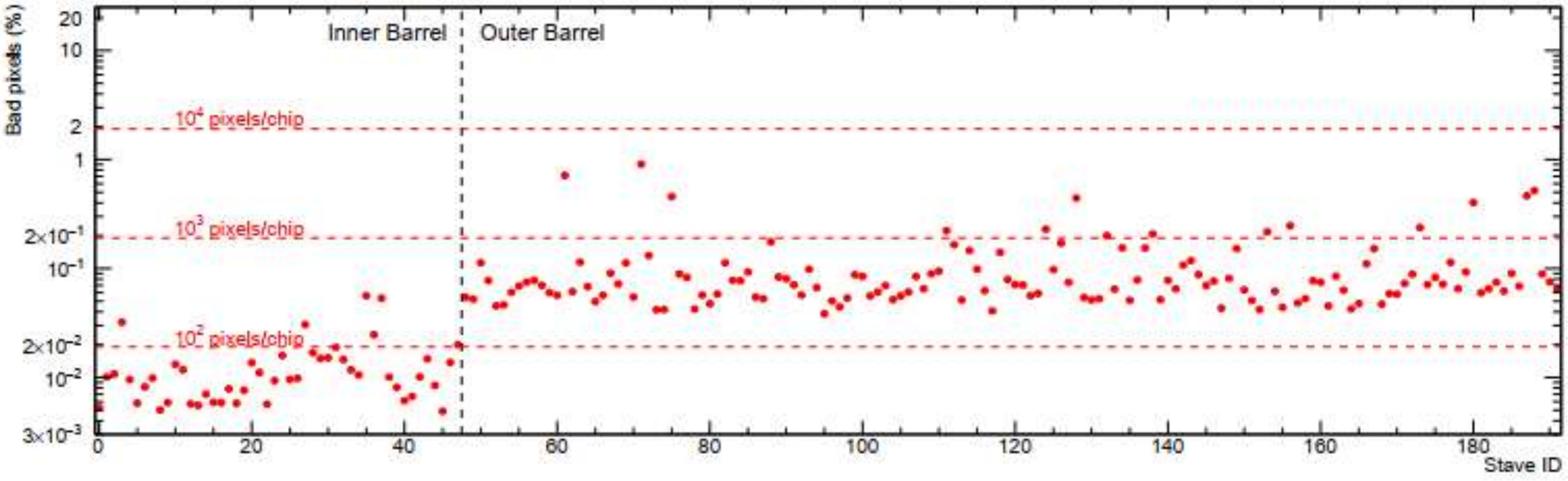
Tracking

- Excellent performance in both pp and Pb-Pb runs with the current updated detector alignment
  - Good angular distribution of tracks
  - Time-dependent acceptance maps accurately describe acceptance loss in MC simulations





Threshold – bad pixels



Bad pixel

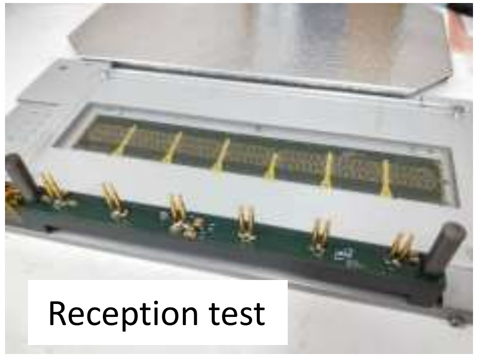
- An excessive noise or a too-low threshold leading to hits independent of the thresholds
- A too-high threshold preventing the pixel from firing with 100% probability within the charge range
- A malfunction in the charge injection circuit preventing the pixel from being stimulated
- A malfunction in the pixel or its respective readout circuitry

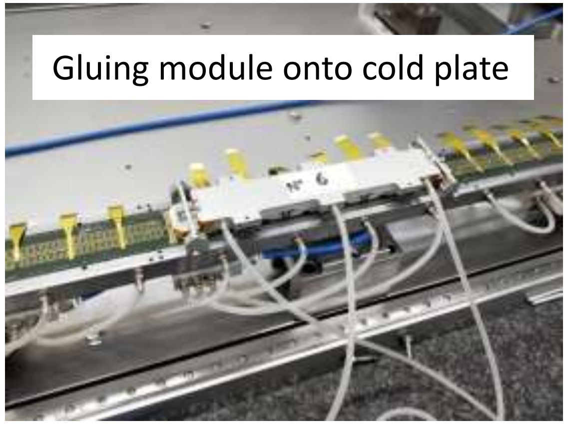
ITS2 has about 1.32×10^7 bad pixels which corresponds to about 0.10% of the total number of pixels.

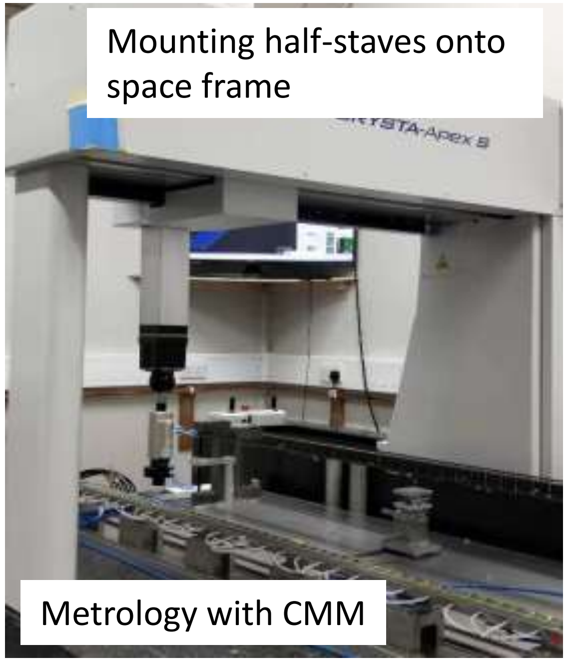
Detector Construction

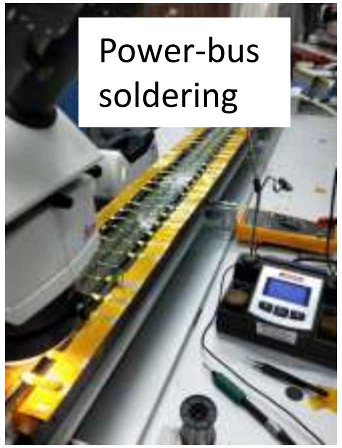
Outer Barrel Stave assembly for ALICE ITS2 in Daresbury Laboratory

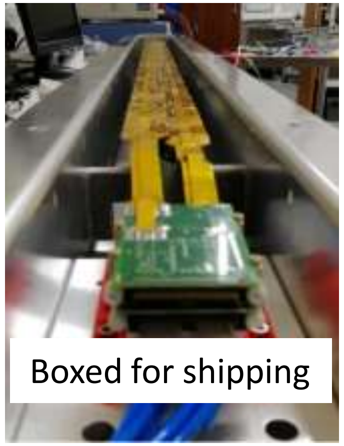
- Achieved one of the highest production yields for the OB staves (95%) across all international staves assembly sites

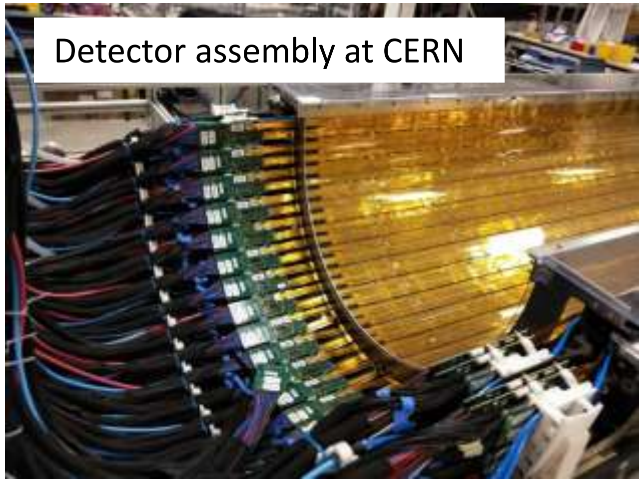












CMM: Coordinate-measuring machine

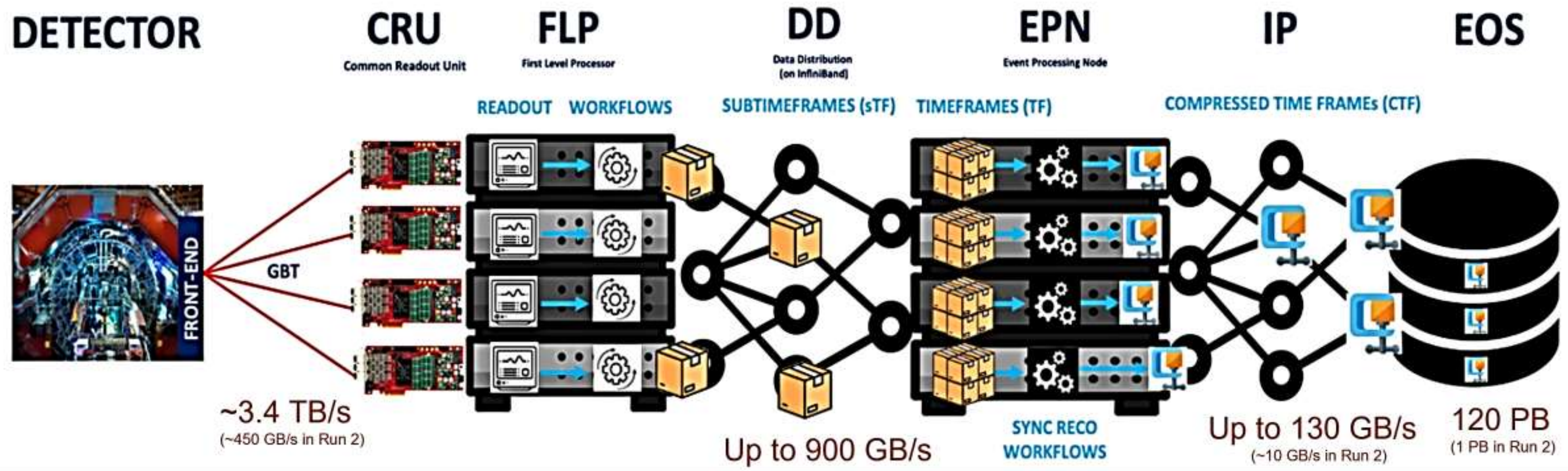
*Performance of the ALICE upgraded inner tracking system, **J. Liu**, JINST 17 (2022) 04, C04032*

Online/Offline (O^2)

Targeting to record large minimum-bias sample

- All collisions stored for main detectors with continuous readout in combination with triggered detectors
- Extreme online data compression (~3.4 TB/s → ~0.1 TB/s) → GPUs to speed up online (and offline) processing

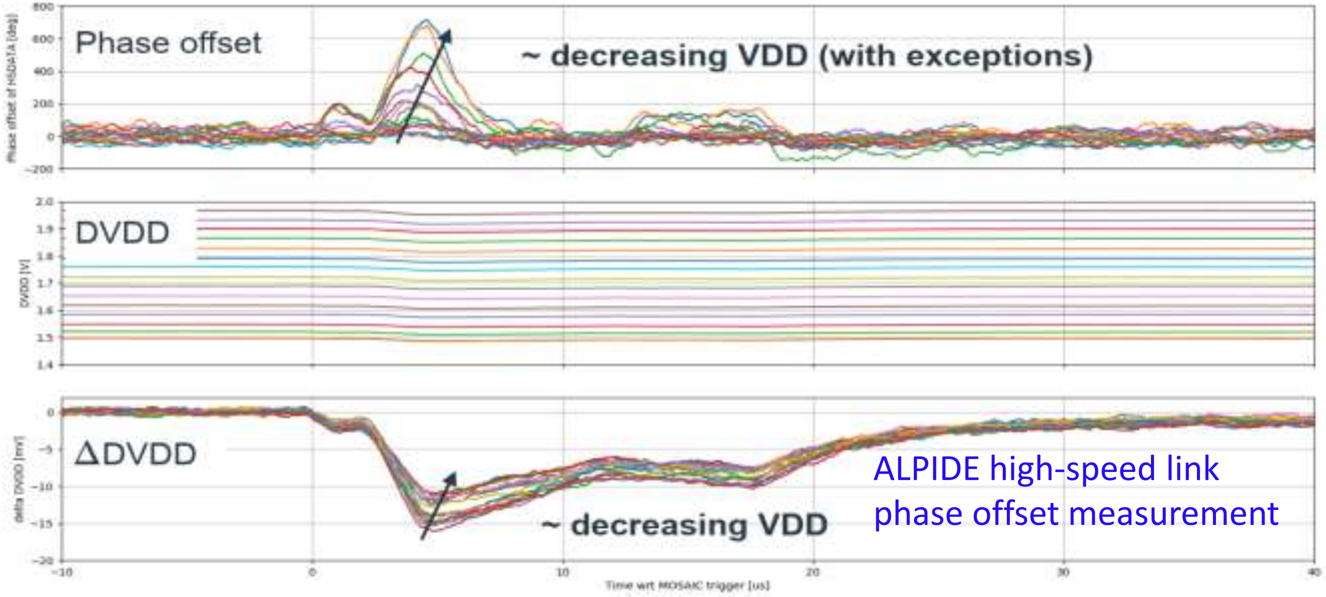
- First level processors (FLP)
  - Readout of detectors (3 TB/s) and raw data processing
  - 200 nodes in total
- Event processing nodes (EPN)
  - Synchronous/asynchronous event reconstruction
  - 280 nodes each with 8 GPUs (extending to 350 nodes)



Lessons learned – high-speed link

- High-speed (HS) link stability
  - For ALPIDE, an independent power domain is dedicated to the high-speed link phase locked loop (PLL), but lacks a low-drop-out (LDO) regulator
  - On modules, no space to route an independent power domain to the PLL, allowing only specific decoupling to the bonding pad → supply voltage fluctuations in other domains are seen by the PLL
  - Significant phase shifts on the HS link can result from supply voltage variations, particularly at the start of high-occupancy event readouts → potentially causing the RU's phase tracking to lose lock
  - Mitigation
    - Gradually increasing the trigger frequency at the start of a run, which also increases power consumption, helps stabilize the link
    - Auto recovery in DCS

In ITS3, LDO regulators will be implemented for high-speed links and independent supply domains will be routed to the detector



ALPIDE high-speed link phase offset measurement

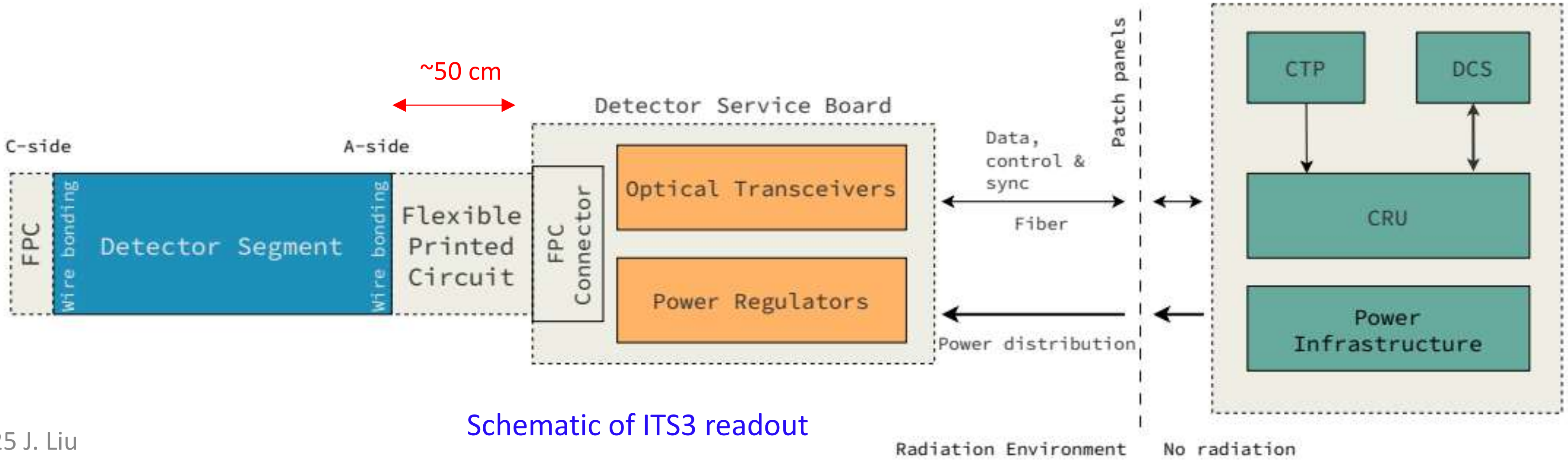
Lessons learned – data protocol and powering

- Data protocol
  - The ALPIDE protocol resynchronization firmware is complex → involving DCS suspending triggers to ALPIDEs, clearing data paths, and reconfiguring both the ALPIDE and RU → a time-consuming process (~10 s)

In ITS3, data protocol will be adapted to facilitate re-synchronization, with added information at the cost of some efficiency

- Powering
  - Voltage drops along the long cables can be compensated but complicate operations
    - Voltage must be reduced before resetting or stopping the clock to avoid exceeding absolute maximum ratings
    - Chip power consumption varies based on operational mode, requiring re-tuning, for example, prior to initiating triggers

Moving last stage of regulation significantly closer for ITS3 → significantly reduced voltage drops



Schematic of ITS3 readout