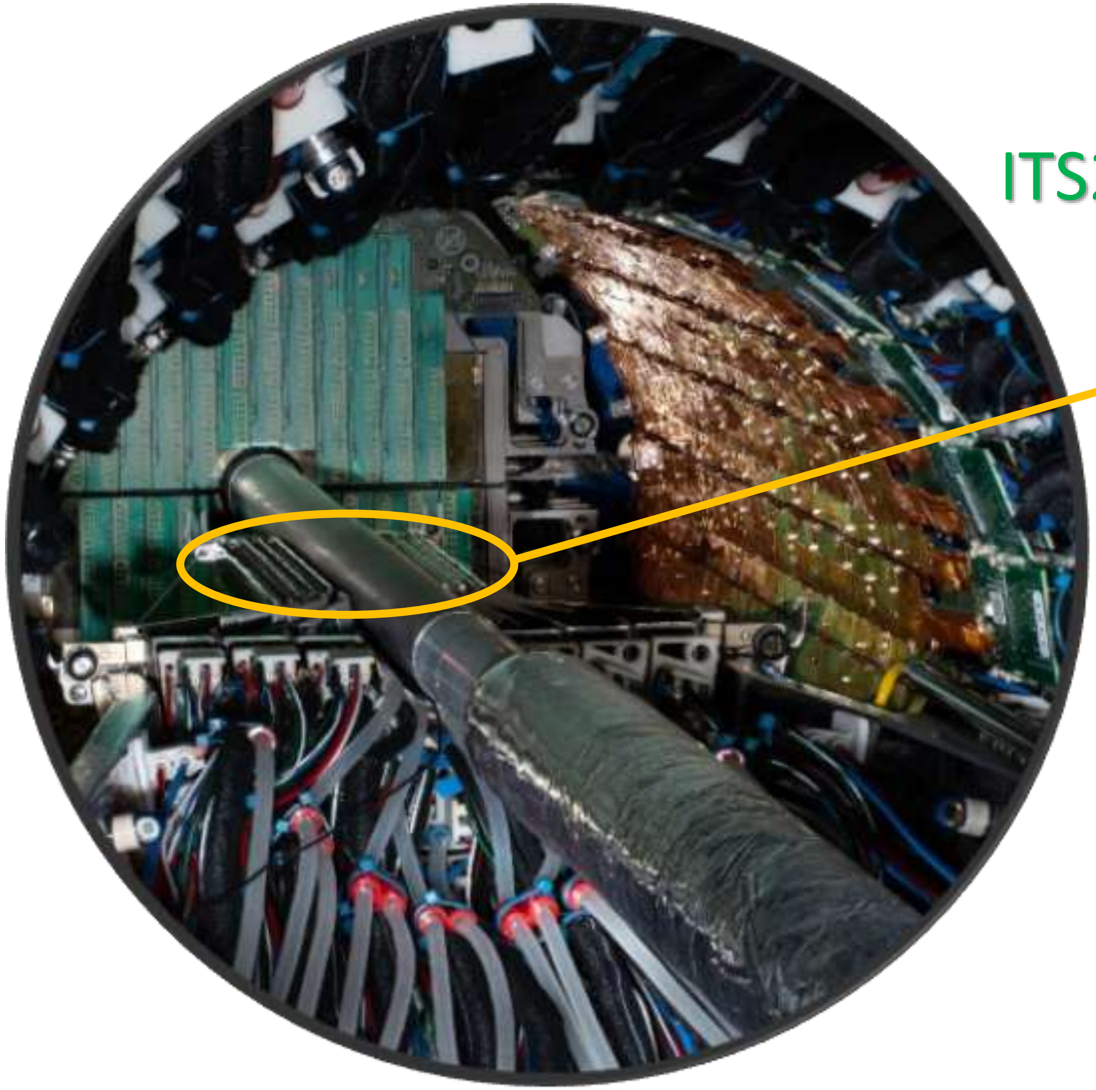
首届ALICE实验与重离子物理讲习班
The 1st ALICE Experiment and Heavy-Ion Physics School



ALICE Inner Tracking System 3: Motivation, concept and R&D

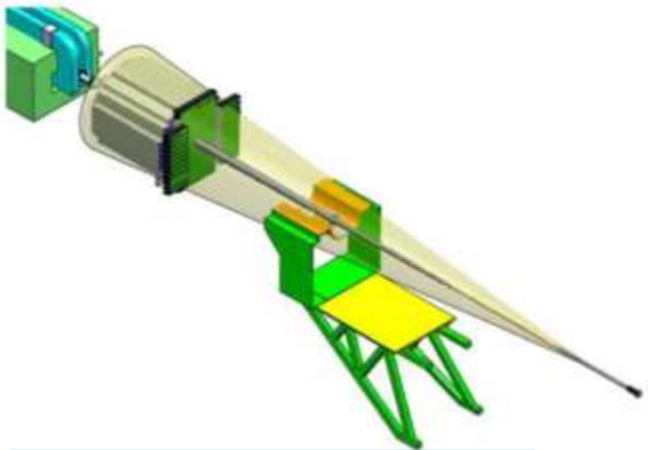
Jian Liu (刘剑)
University of Liverpool

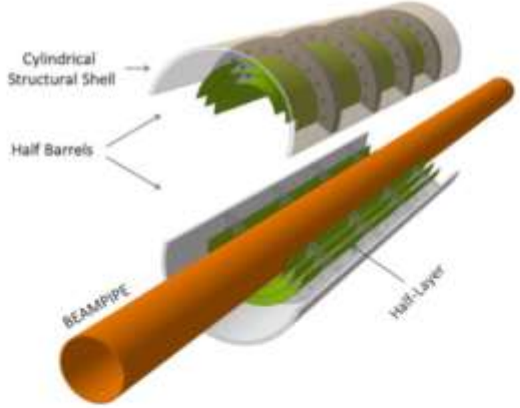
3 - 10 November 2025 | Fudan University, Shanghai, China

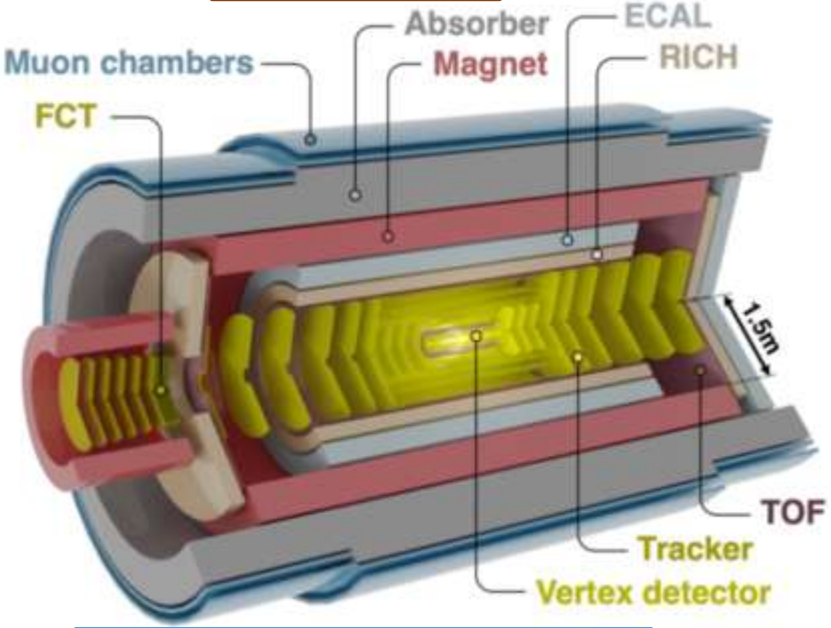
ALICE upgrades timeline

LS3: FoCal and ITS3

LS4: ALICE 3







FoCal LoI: CERN-LHCC-2020-009
FoCal TDR: ALICE-TDR-022

Not covered in this talk

ITS3 LoI: CERN-LHCC-2019-018
ITS3 TDR: ALICE-TDR-021

ALICE 3 LoI: CERN-LHCC-2022-009

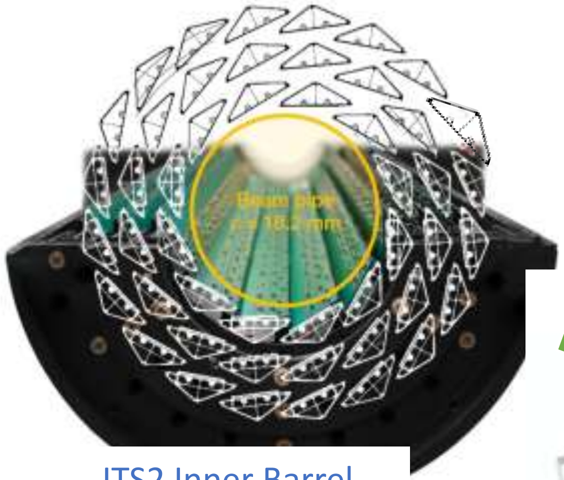
Not covered in this talk

ITS3

Replacing the 3 innermost layers with new ultra-light, truly cylindrical layers

- Wafer-scale bent sensors (1 sensor per half-layer) in 65 nm technology
- Reduced material budget (from 0.36% to 0.07% X_0 per layer) with a highly homogenous material distribution by removing water cooling, circuit boards and mechanical support
- Closer to the interaction point (from 23 to 19 mm)

Better vertexing and lower backgrounds for heavy-flavour and low-mass dielectron studies

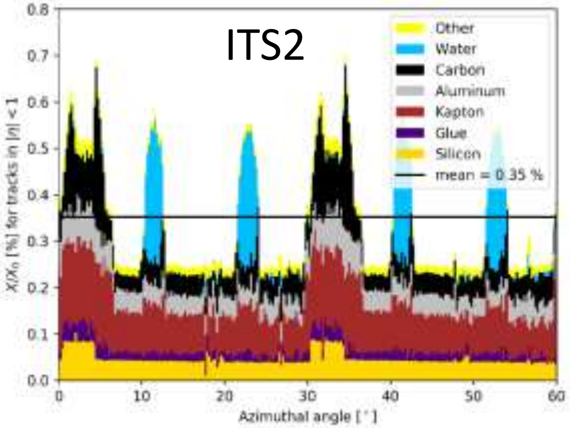


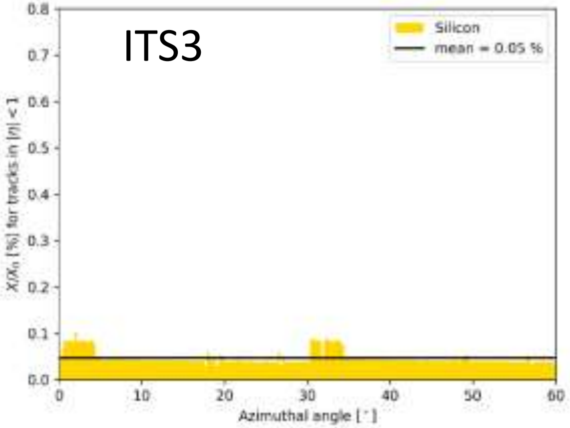
ITS2 Inner Barrel

ITS3

Radiation tolerance

- TID: 400 krad
- NIEL: 4×10^{12} 1MeV n_{eq} /cm^2





IB Layer Parameters	Layer 0	Layer 1	Layer 2
Sensor length [mm]		265.992	
Sensitive length [mm]		259.992	
Sensor azimuthal width [mm]	58.692	78.256	97.820
Radial position [mm]	19.0	25.2	31.5
Equatorial gap [mm]		1.0	
Max thickness [µm]		50	

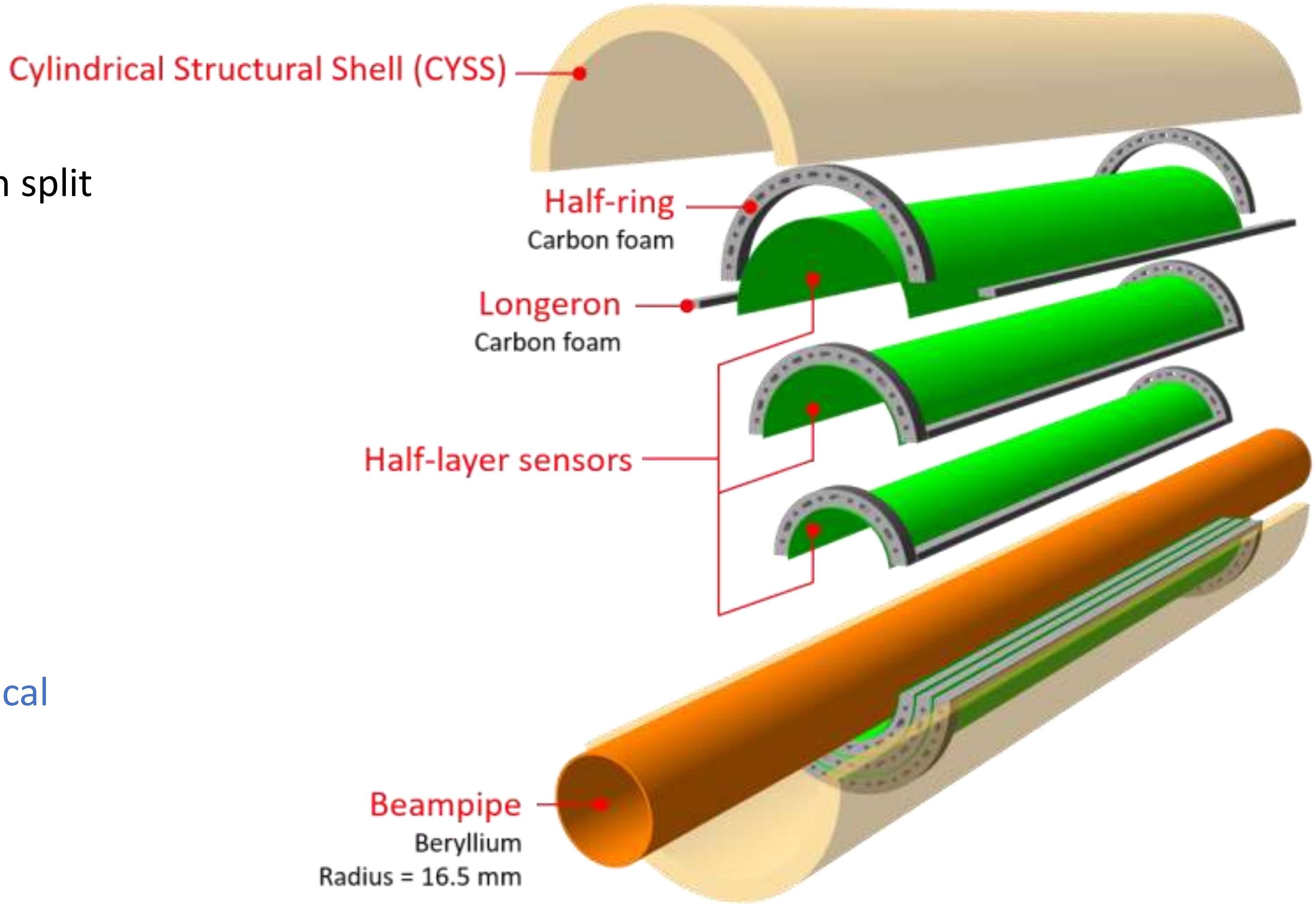
Table 3.3: Design dimensions of the sensor dies and radial position.

Detector concept

- Three cylindrical detector layers, each split into two half-layers

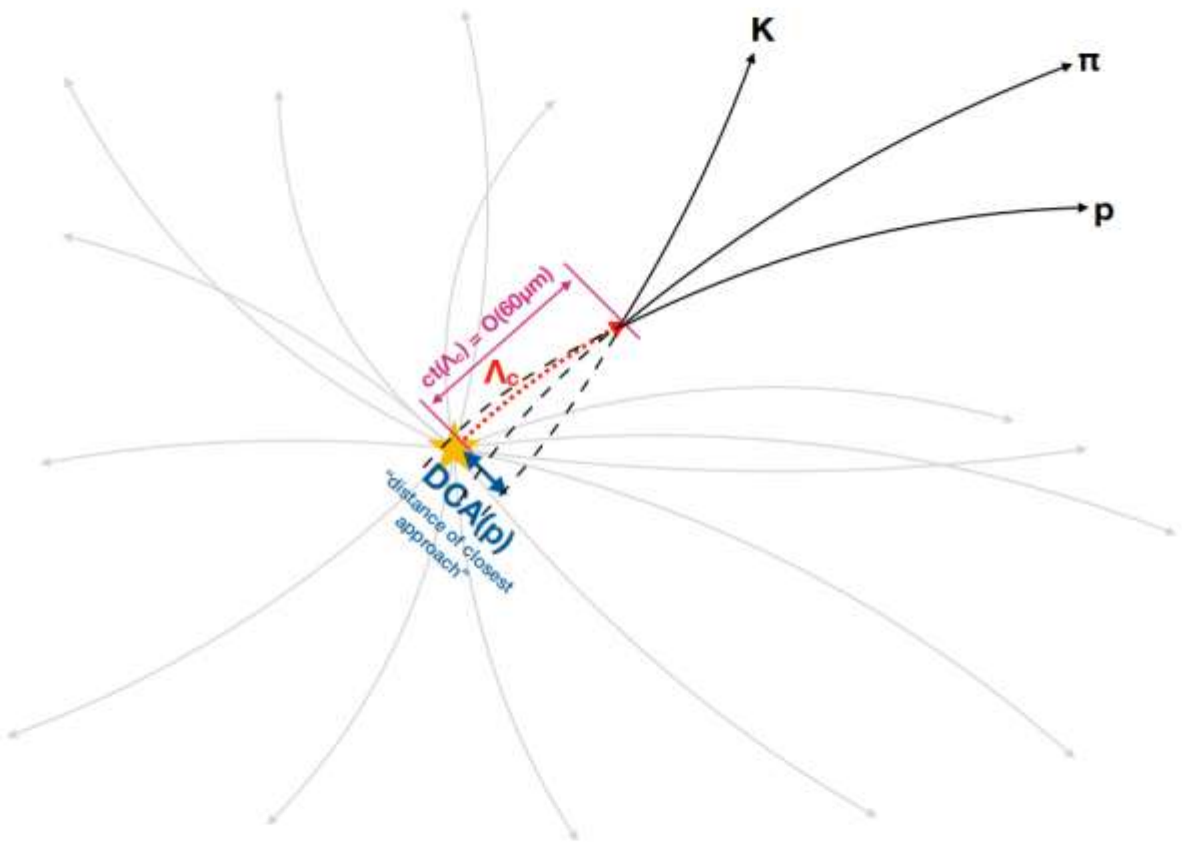
- Each half-layer includes
  - Wafer-scale bent silicon sensor
  - Flexible printed circuits (FPC)
  - Lightweight carbon foam structures
  - Polymer gas distributor

- All layers are enclosed by the CYlindrical Structural Shell (CYSS)



Λ_c reconstruction: a test case for vertexing

A benchmark for secondary-vertex performance - a short-lived charm baryon with cτ ≈ 60 μm



Challenge

- In a central Pb–Pb collision, O(10k) charged particles are produced.
- Random combinations of p, K, π tracks form a huge combinatorial background

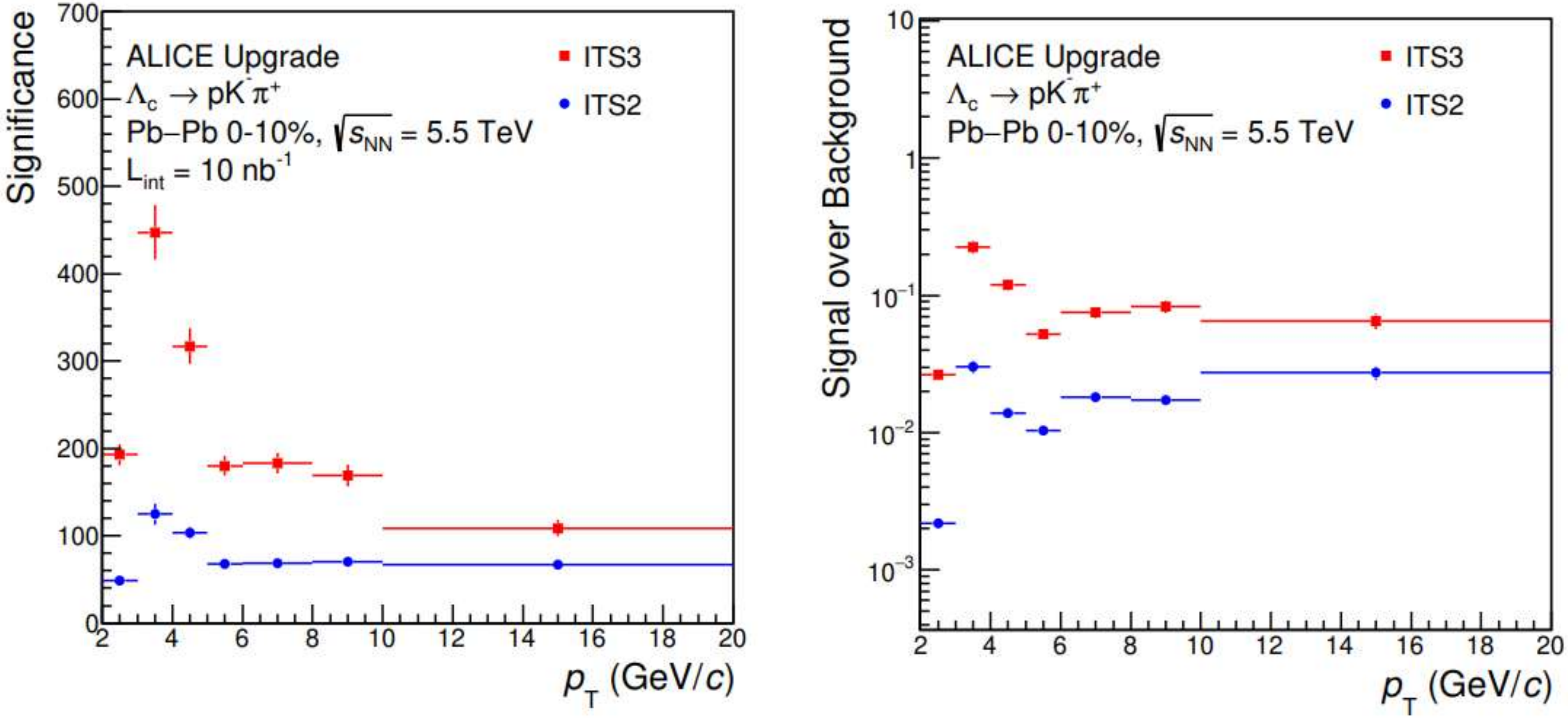
Background suppression

- Particle identification (PID)
  Use TPC + TOF to select proton, kaon, and pion tracks
  → Strongly reduces random combinations, since most tracks are pions while protons and kaons are relatively rare

Topology

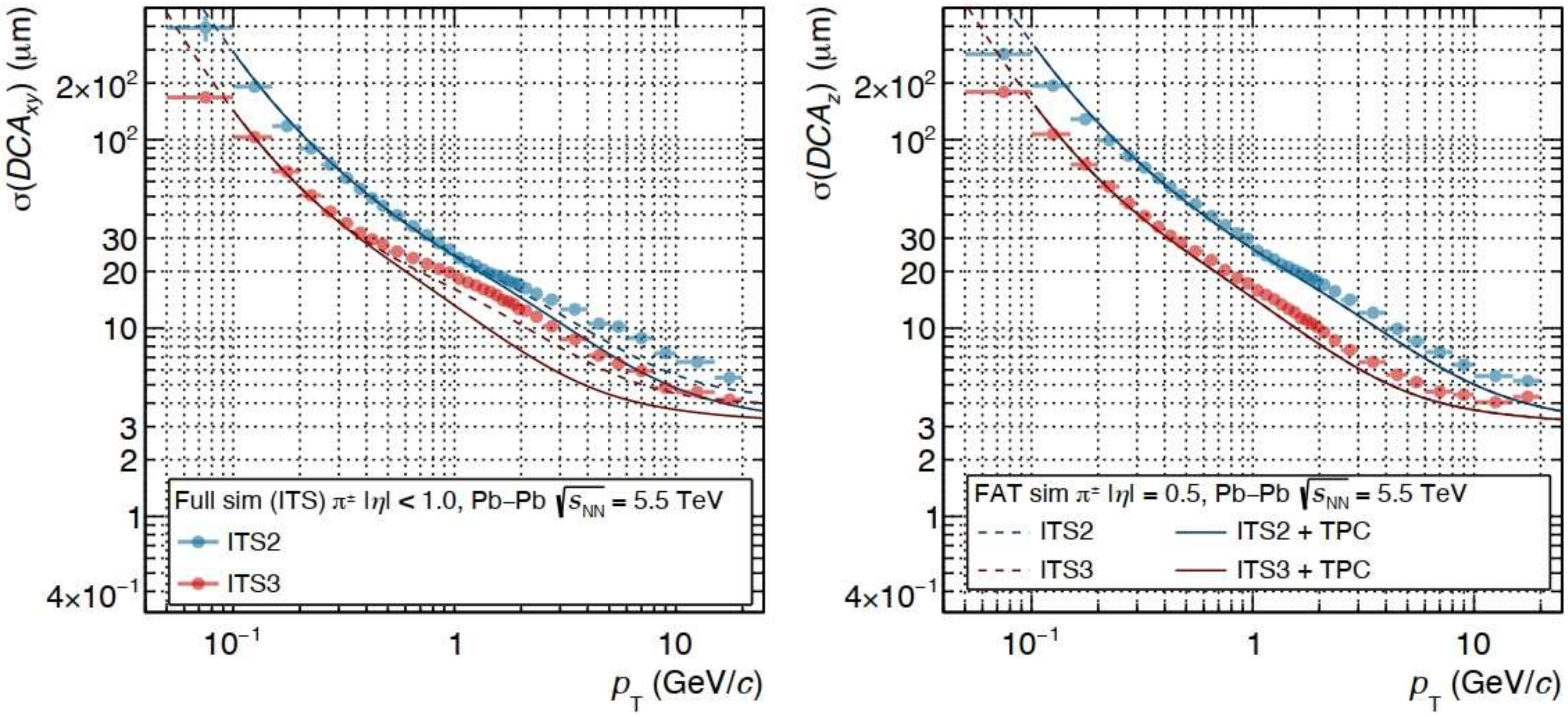
- Λ_c daughters have non-zero DCA to the PV (displaced tracks)
- Apply minimum DCA cuts on single tracks to reject primary particles
- Combine displaced tracks to fit a common secondary vertex separated from the PV
- These topological cuts isolate genuine Λ_c decays

Λ_c reconstruction: impact of ITS3 performance



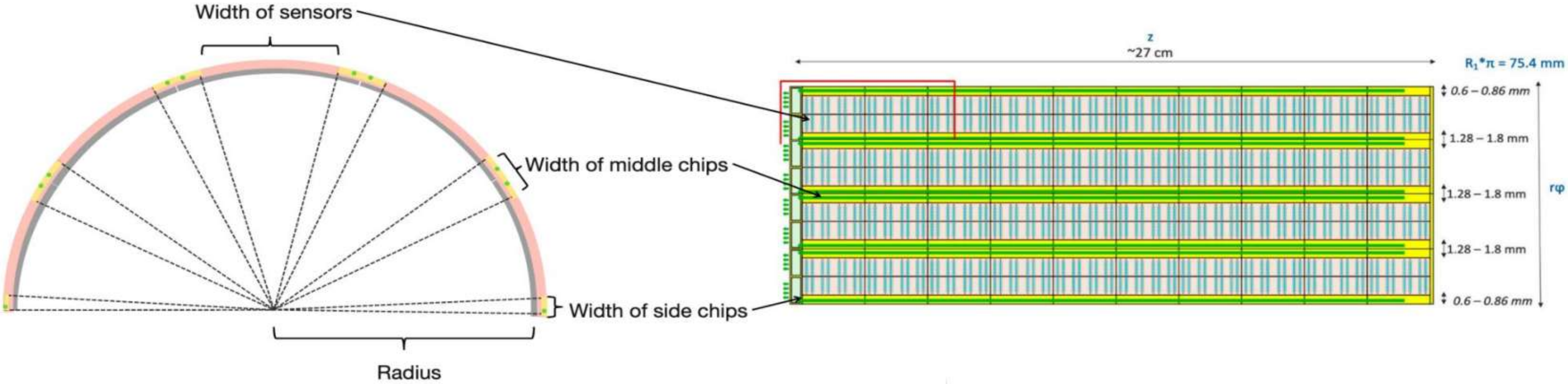
- ITS3 provides factor ~ 3–4 higher signal significance, especially at low p_T
- Signal-to-background ratio improves by nearly one order of magnitude

Performance – pointing resolution

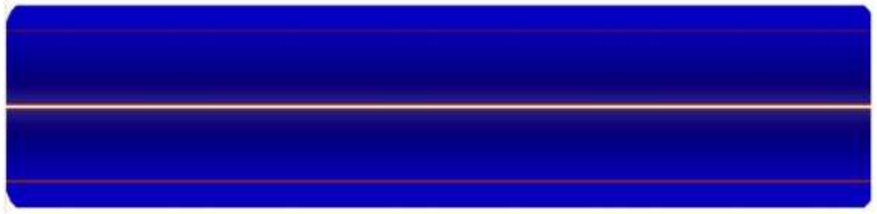


- Improvement in pointing resolution by a factor of 2 over all momenta → improved separation of secondary vertices

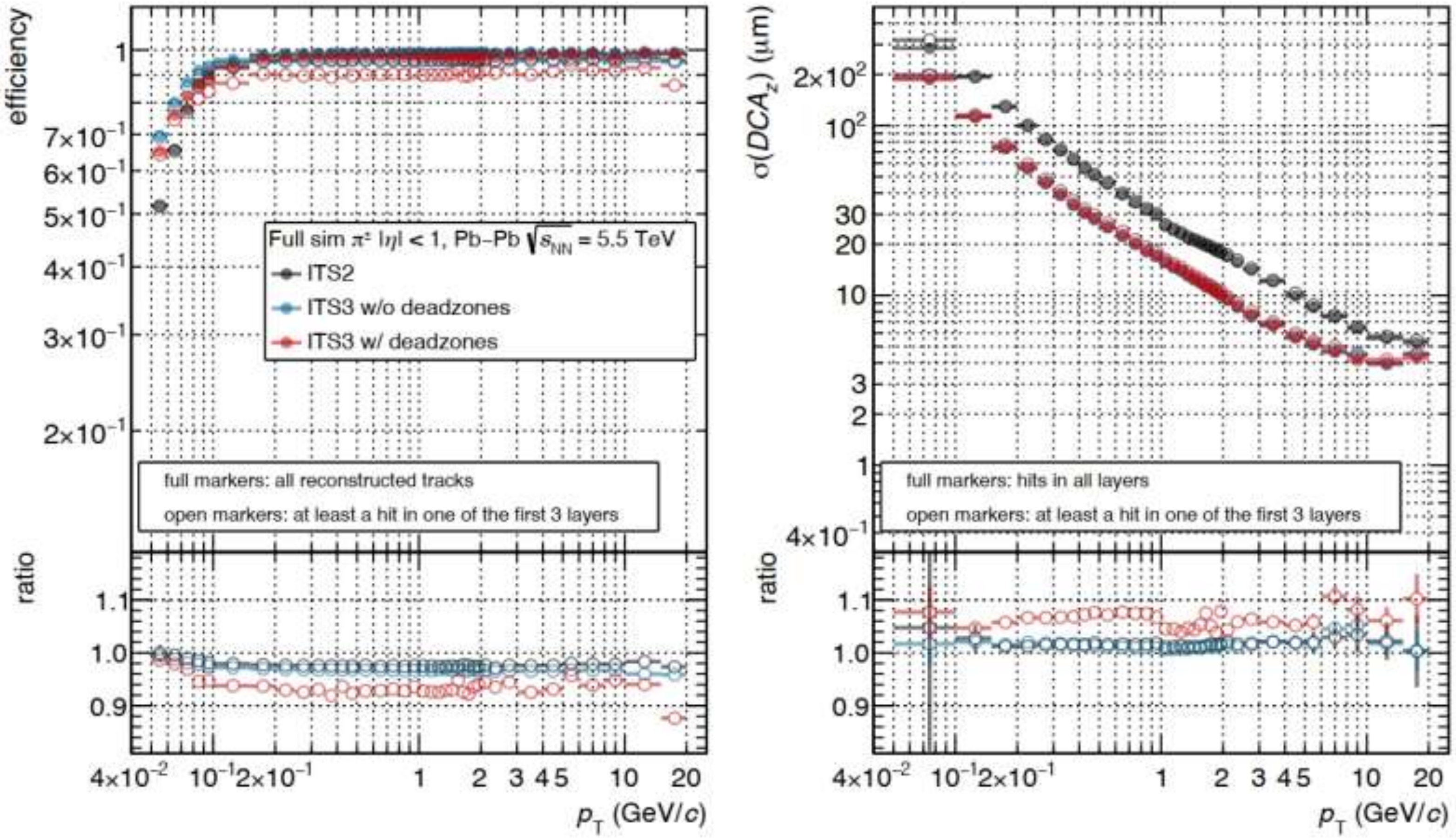
ITS3 geometry - dead zones



- Blue: sensitive areas
- Red: dead areas
- Gap between the two hemicylinders



Performance – impact on dead zones



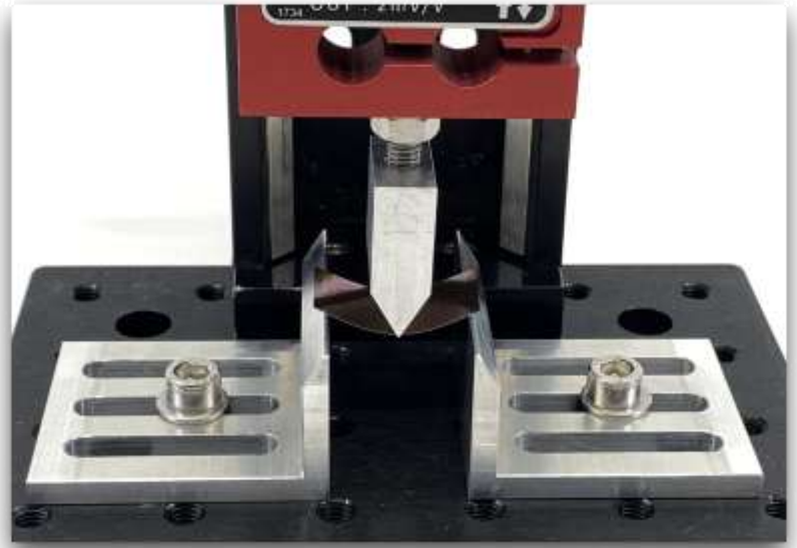
Assumptions here:

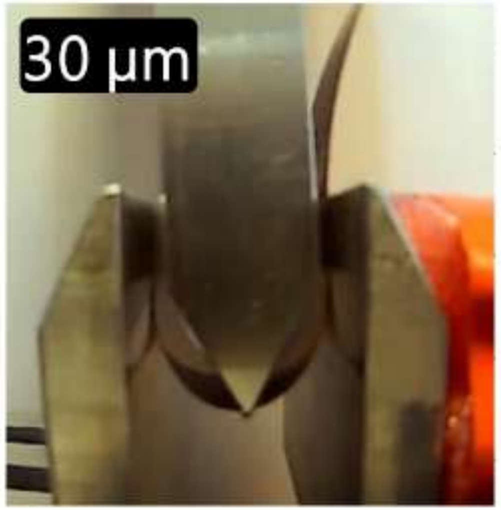
- 1 mm gap between top and bottom
- Total: 8-9% dead area

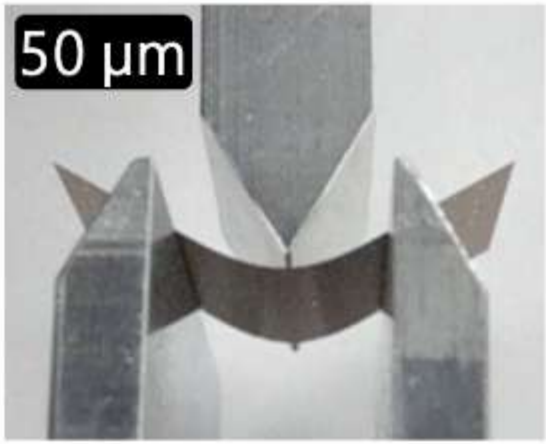
- Increase of tracking efficiency for low-p_T particles and extension of the low-p_T reach
- Dead zones have direct impact on efficiency and pointing resolution → important to optimise mechanics and chip design in this parameter

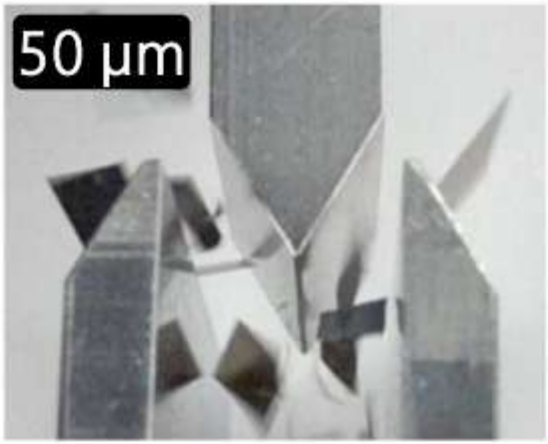
Can we bend silicon?

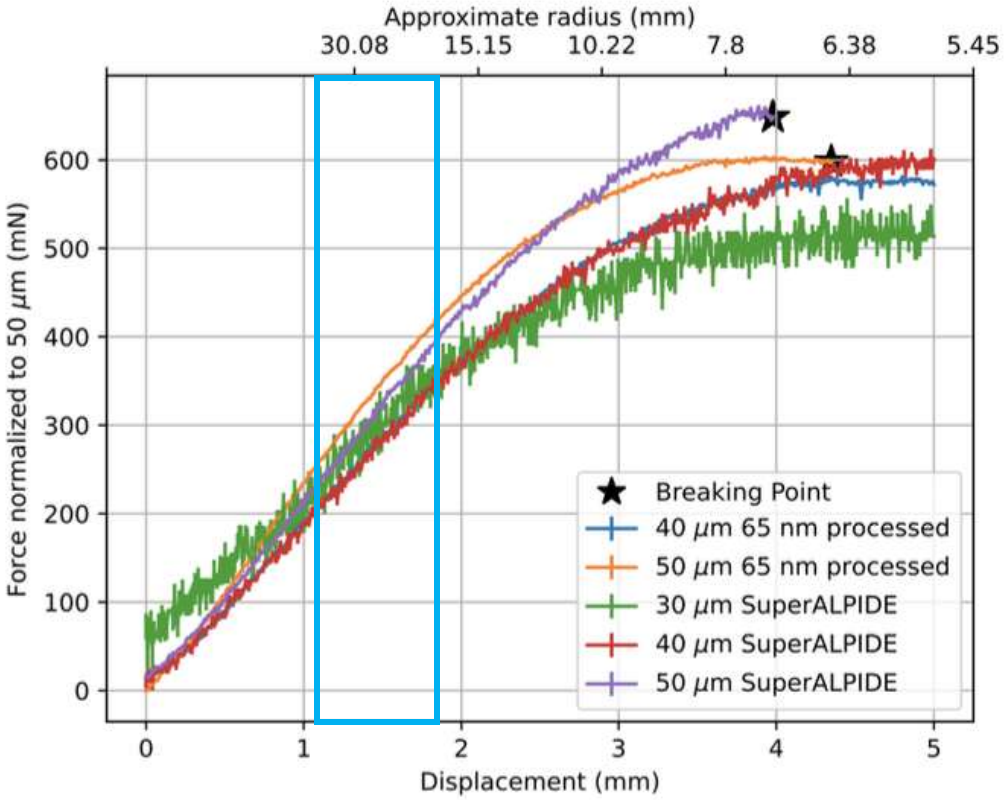
- Thin MAPS are very flexible
- Bending force proportional to $(\text{thickness})^{-3}$
- ITS3 target radius and thickness verified





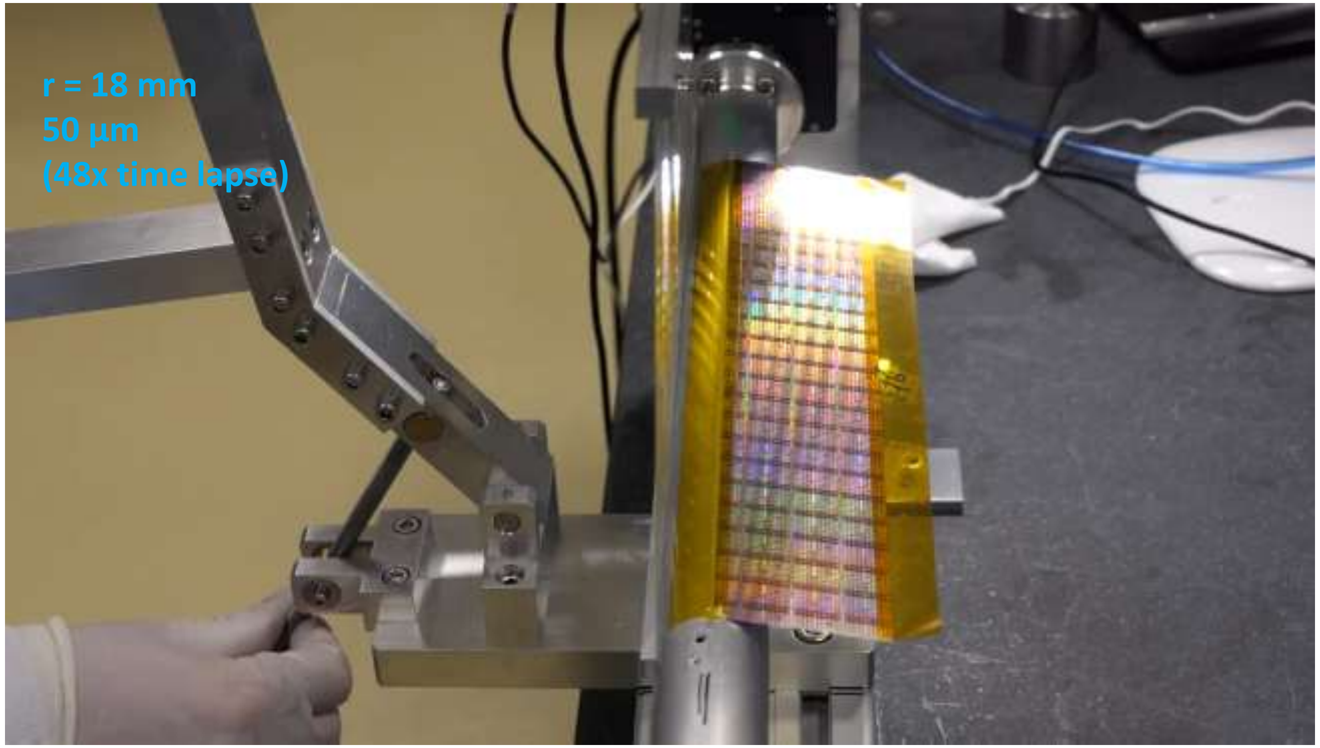




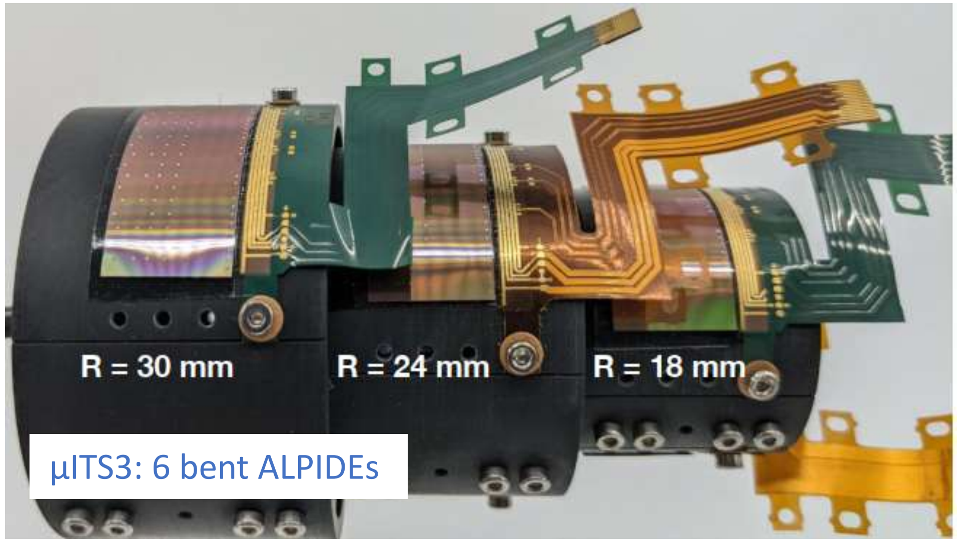


Sensor bending

- Functional chips (ALPIDEs) and MLR1 sensors are bent routinely at different labs
- Bending of ER1 prototypes (babyMOSS) ongoing
- Full mock-up of the final ITS3, called “µITS3”
    - 6 ALPIDE chips, bent to the target radii of ITS3 tested

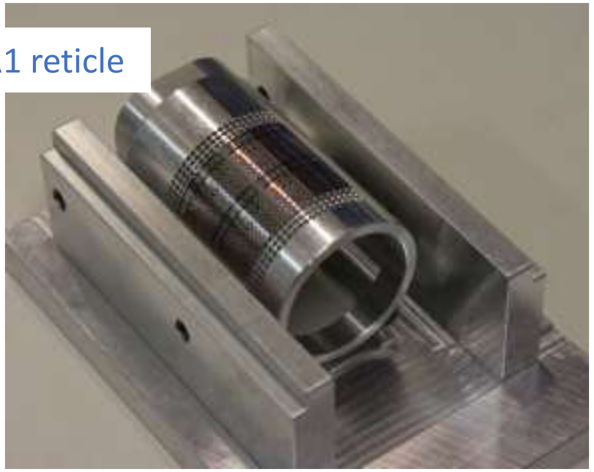


Bending wafer size sensor (using MLR1 wafer)



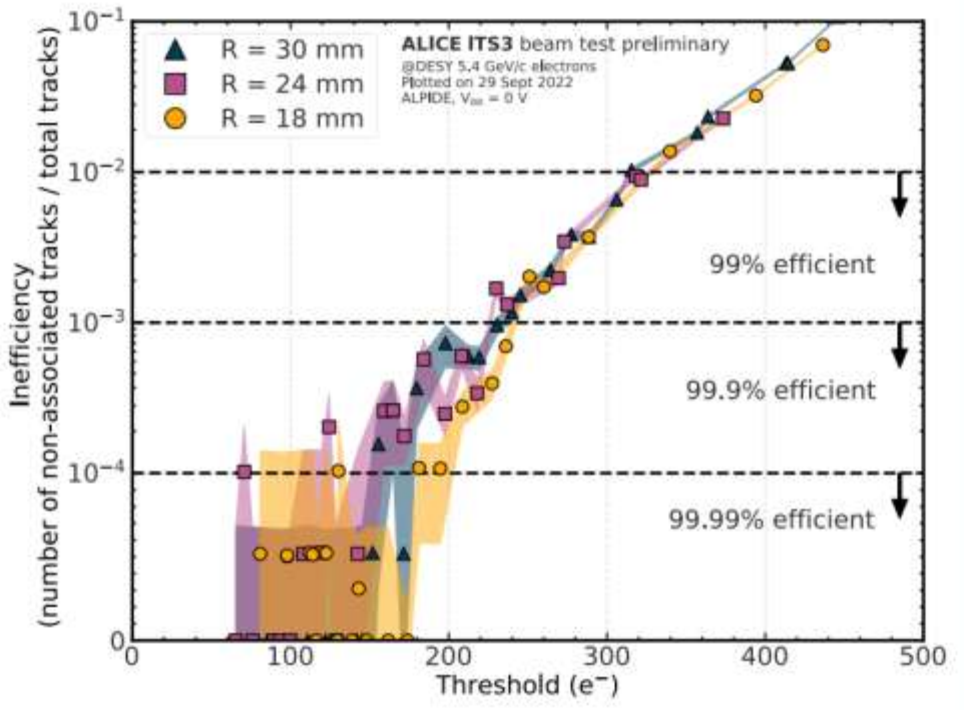
µITS3: 6 bent ALPIDEs

Bent MLR1 reticle

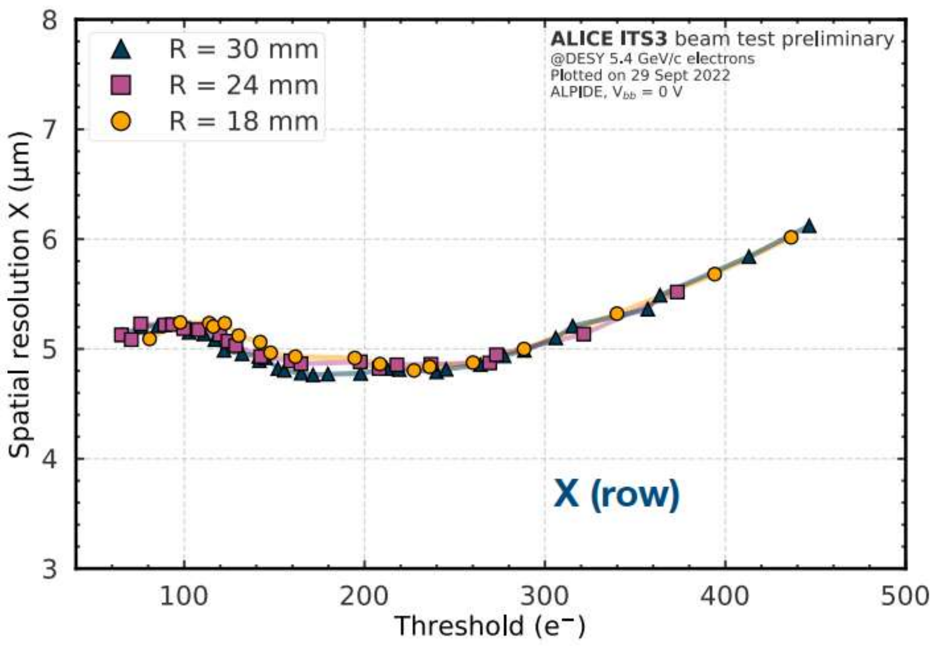


Performance after bending

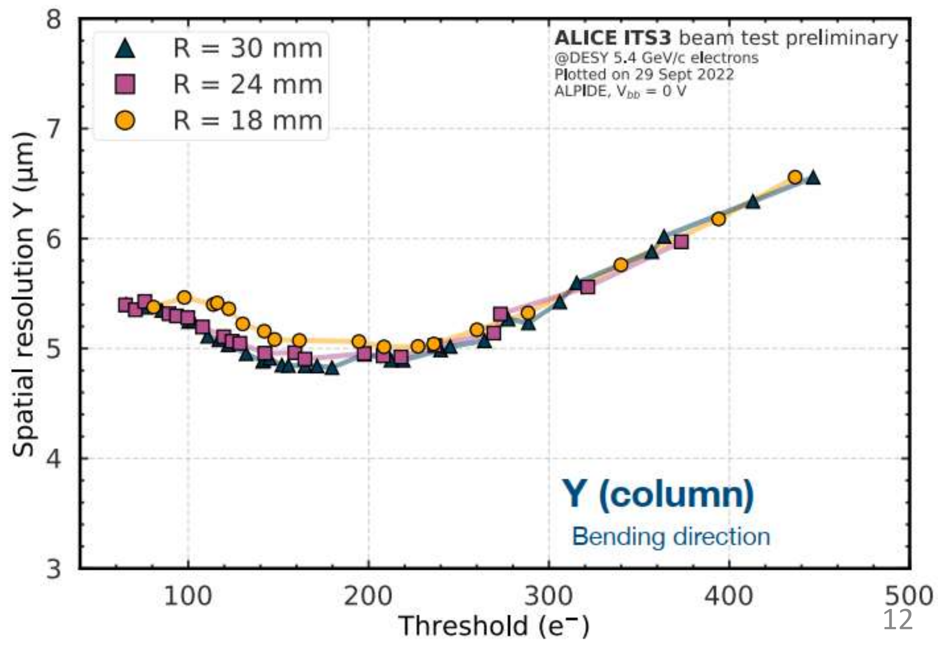
- Sensors remain fully functional after bending
- No performance degradation observed at target bending radius
- Spatial resolution of 5 μm, consistent with flat ALPIDE
- Detection efficiency exceeds 99.99% under nominal conditions, matching performance of unbent ALPIDE



Inefficiency

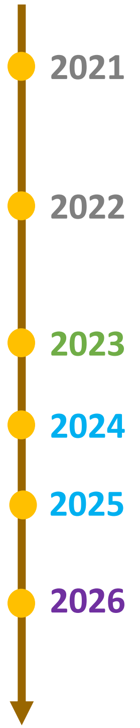


Spatial Resolution



Chip development roadmap

To realize reliable wafer-scale sensors, the design evolves through multiple engineering runs



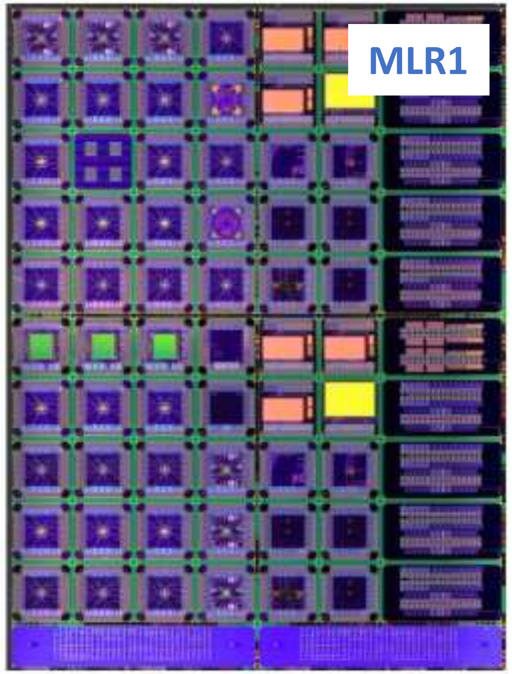
MLR1 (Multi-Layer Reticle 1): first MAPS in TPSCo 65 nm
- Successfully qualified the 65 nm process for ITS3 (and much beyond)

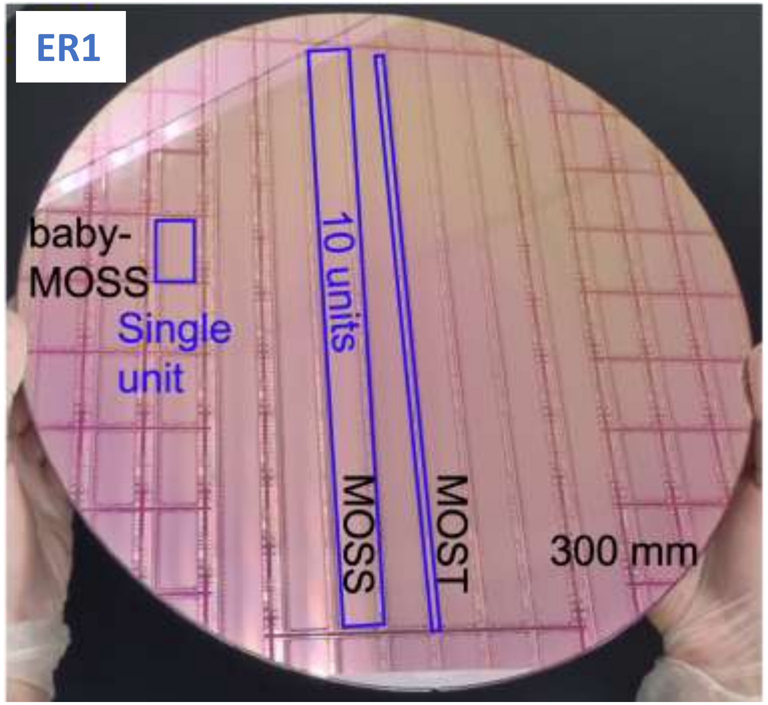
ER1 (Engineering run 1): first stitched MAPS
- Large design "exercise", stitching was new
- Tests concluded mid-2025

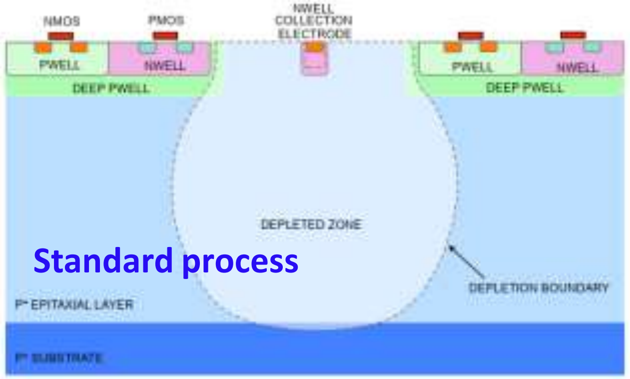
ER2: first ITS3 sensor prototype
- Tape-out in July 2025

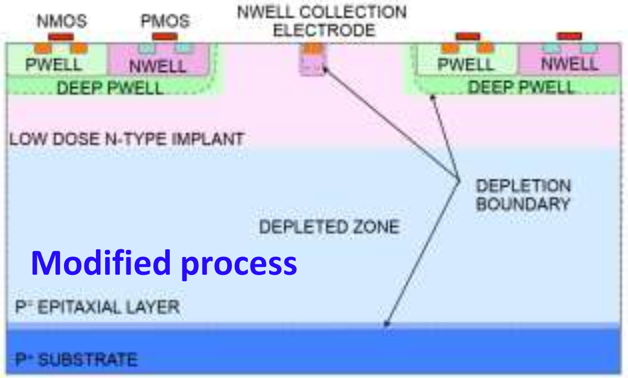
ER2: testing expected early 2026

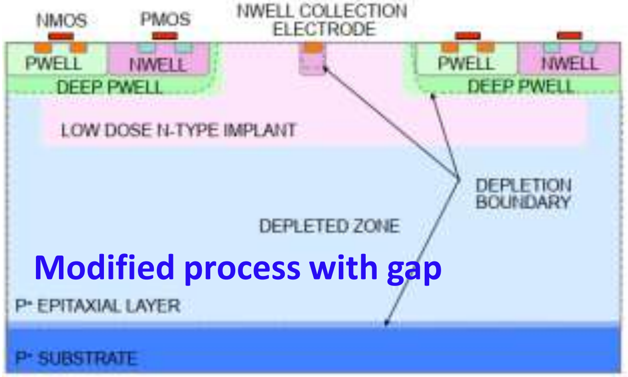
ER3: ITS3 sensor production



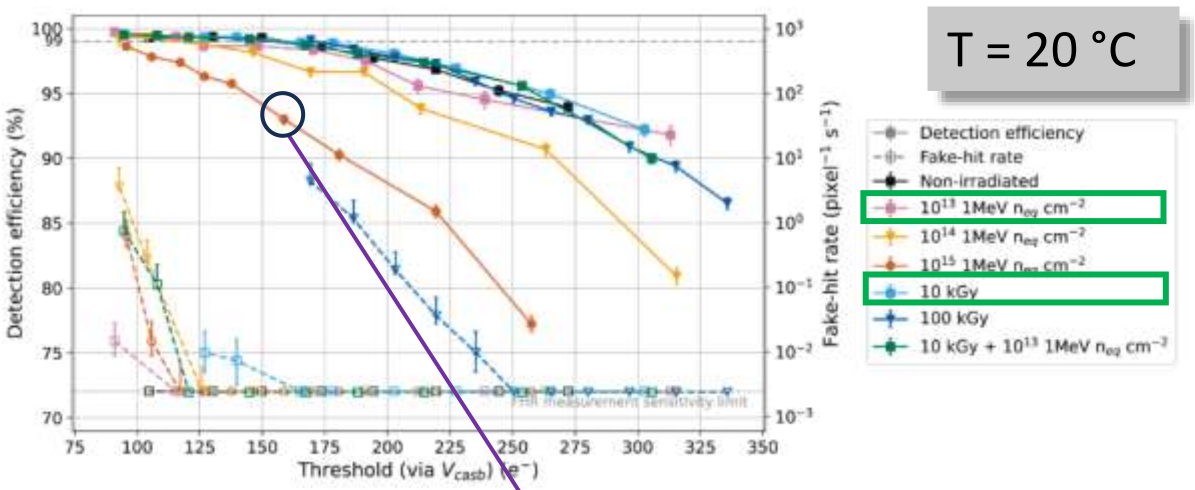


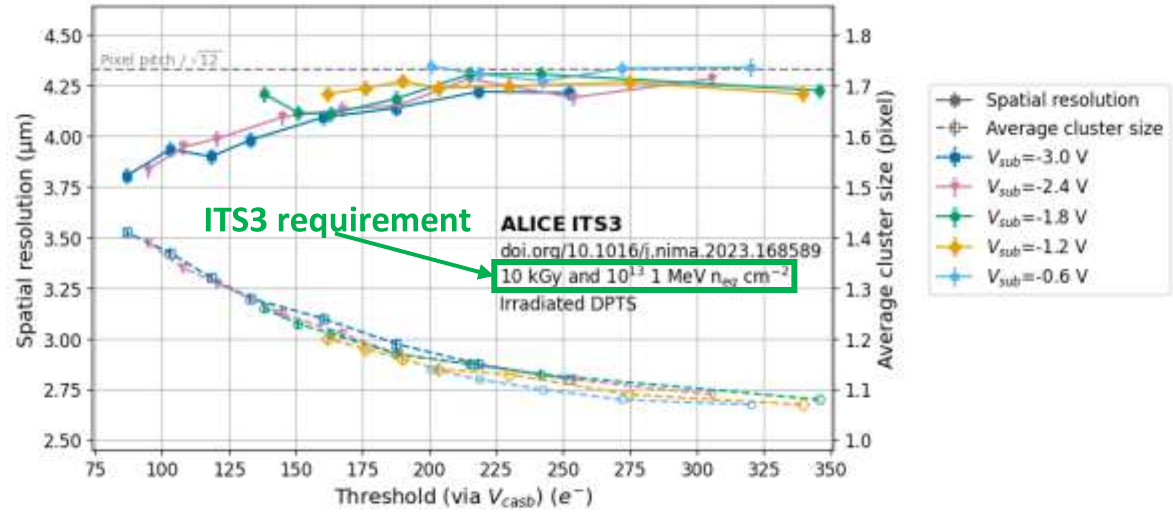


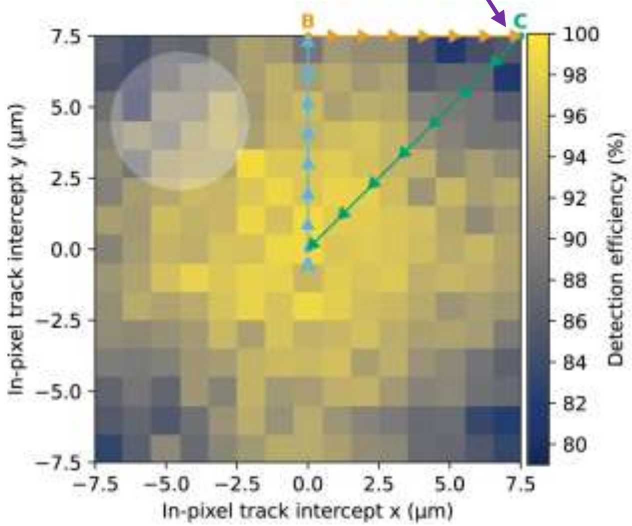


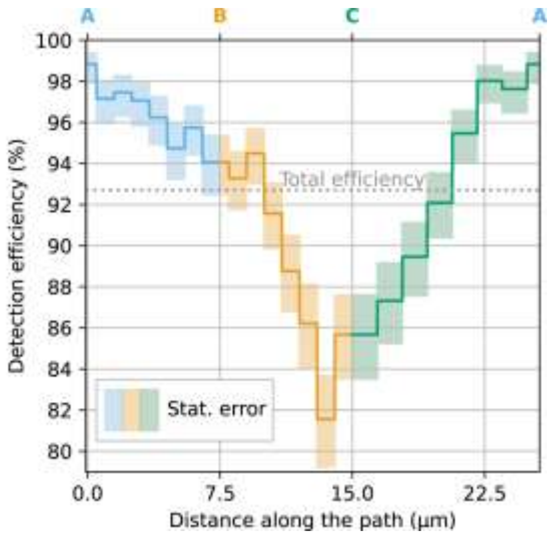


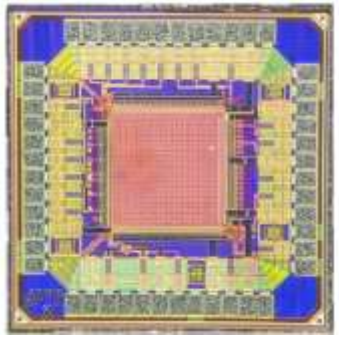
MLR1 characterization (1/2)









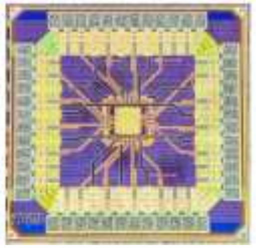


Digital Pixel Test Structure (DPTS)

- 32x32 pixel matrix
- Asynchronous digital readout with Time-over-Threshold information
- Pitch: 15 µm
- Only “modified with gap” process

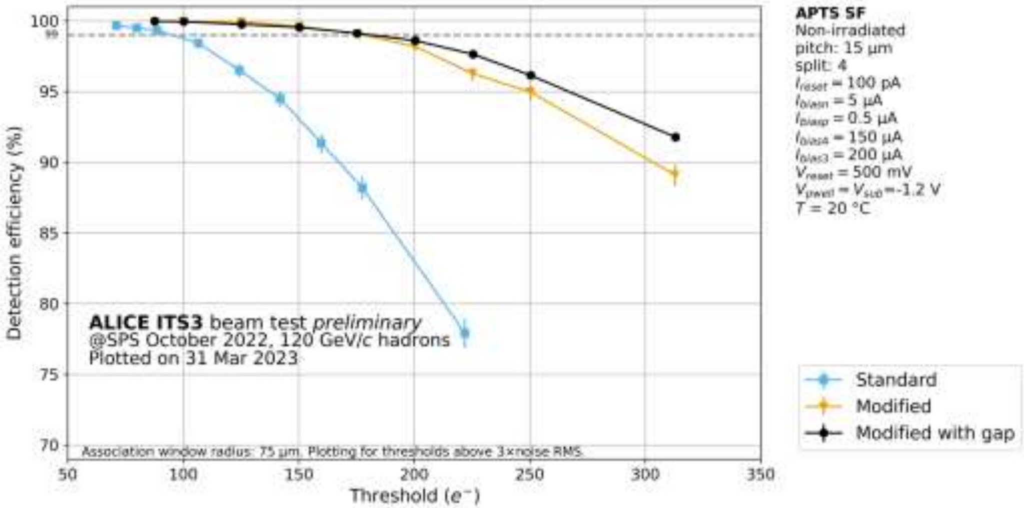
- Efficiency losses predominantly at pixel edges and corners

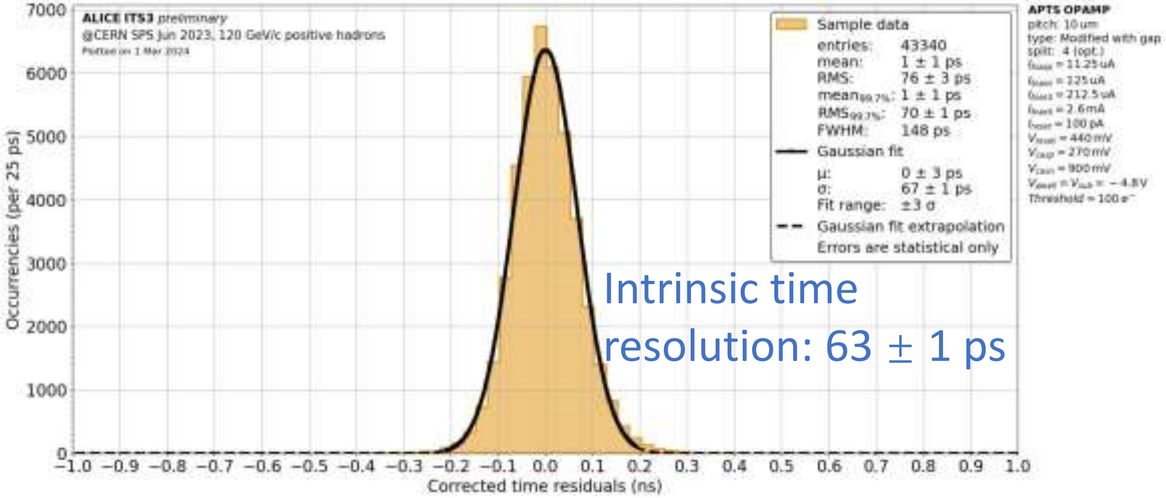
MLR1 characterization (2/2)

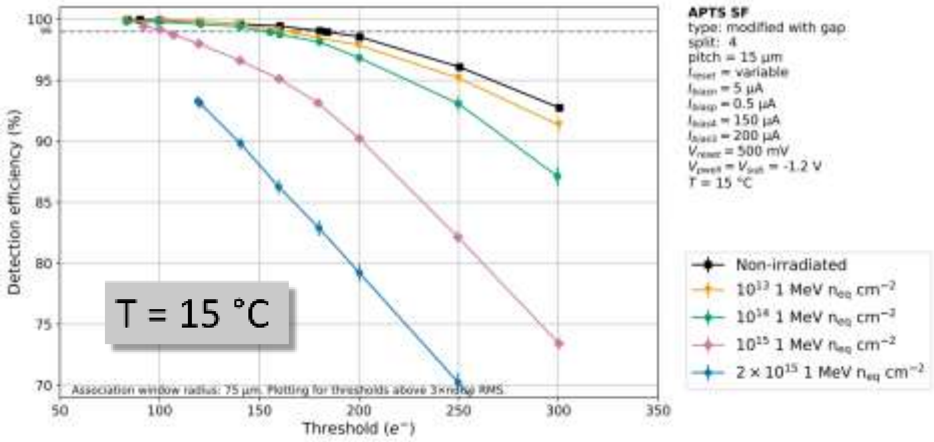


Analogue Pixel Test Structure (APTS)

- 6x6 pixel matrix
- Direct analog readout of central 4x4 pixels
- Two types of output drivers
  - Source follower (APTS-SF)
  - Fast OpAmp (APTS-OA)
- Pitch: 10, 15, 20 and 25 µm



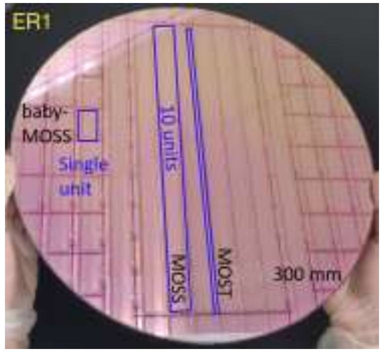




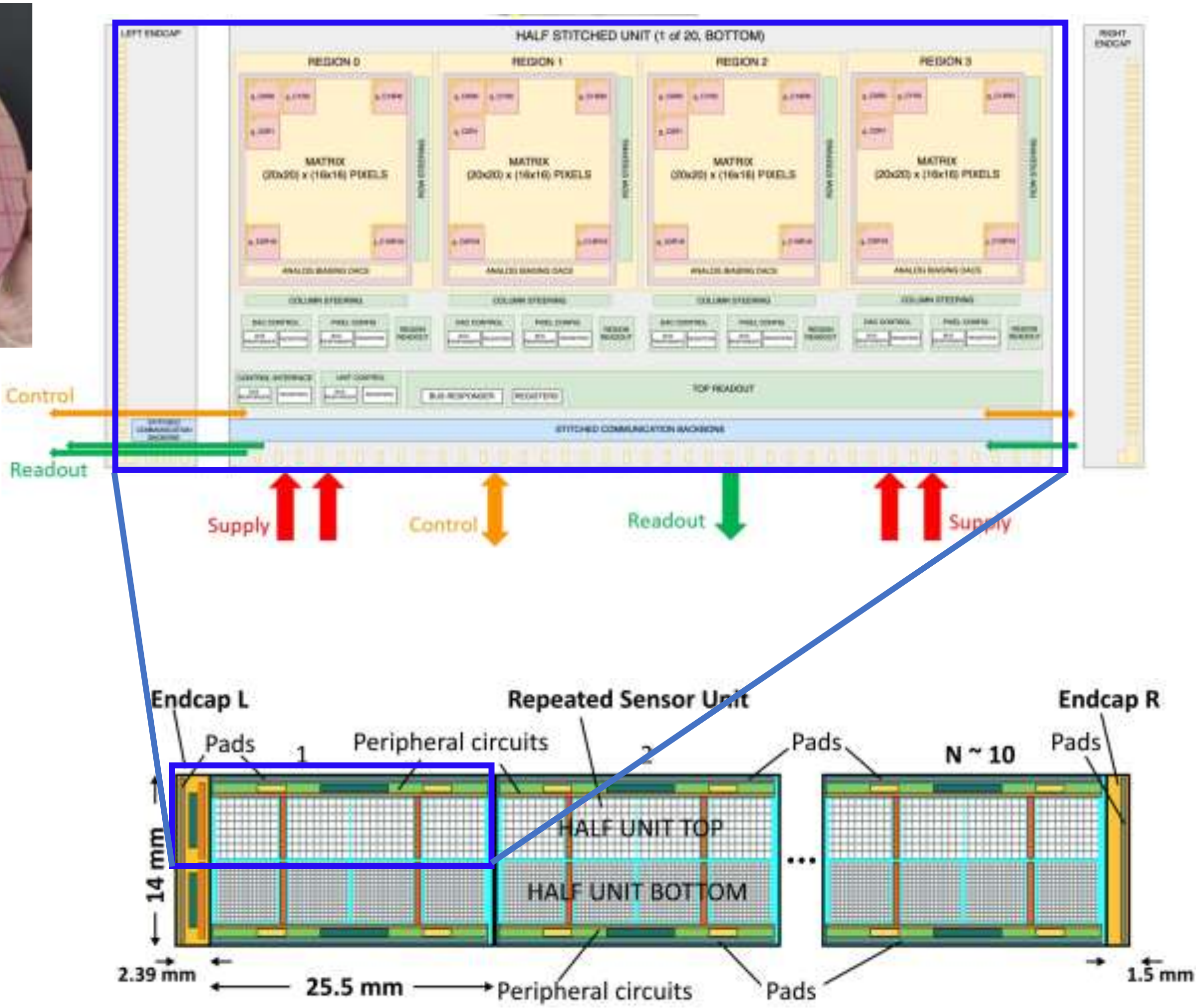
- Validated in terms of charge collection efficiency, detection efficiency and radiation hardness
- Several pixel variants (pitch 10 - 25 µm) were tested both in laboratory and in beam tests
- Excellent detection efficiency over large threshold range for the ITS3 radiation hardness requirement
- Promising also for future applications like ALICE 3 Vertex Detector and FCC-ee

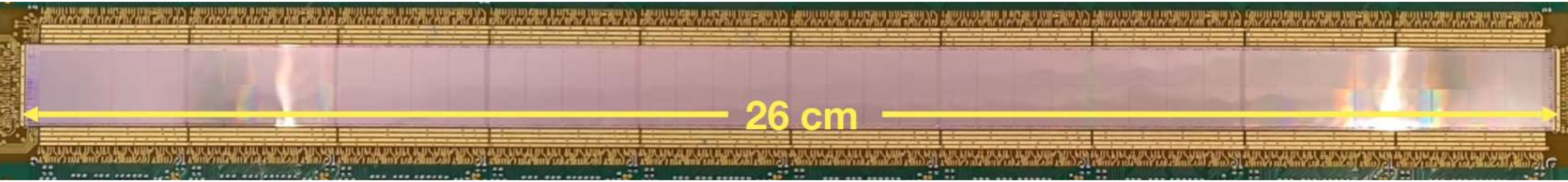
The 65 nm technology qualified!

MOSS



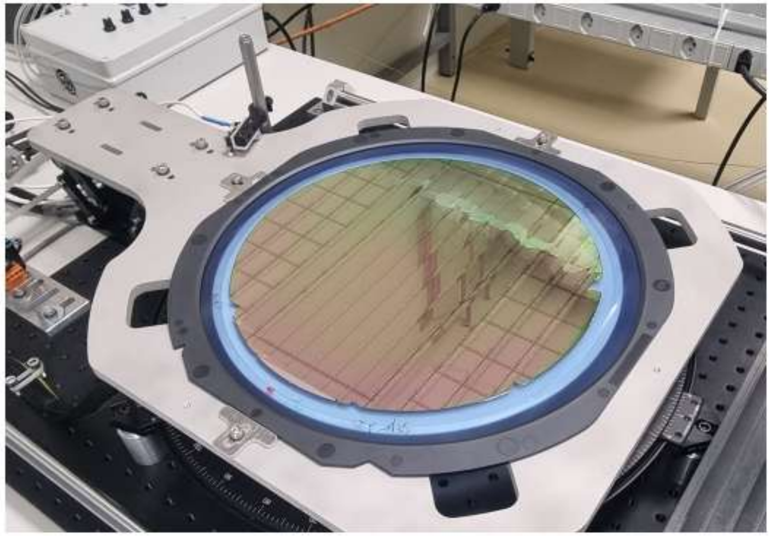
- 14 x 259 mm, 6.72 MPixel
- Segmented into
  - 10 repeated sensor units (RSU)
  - Top and bottom halves with different pitches (22.5 and 18 μm)
  - Four different sub-matrices each with different analog designs
- Each half RSU is powered and can be tested independently
  - Goal: understanding of yields and possible defects
- Stitched "back-bone" allows to control and readout the sensor from the left short side

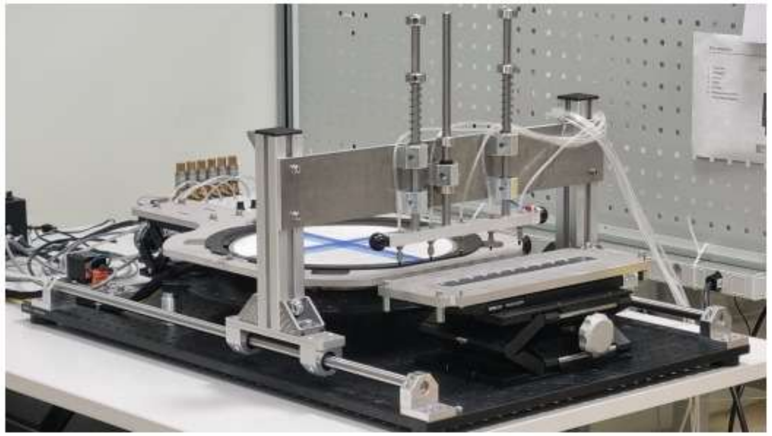


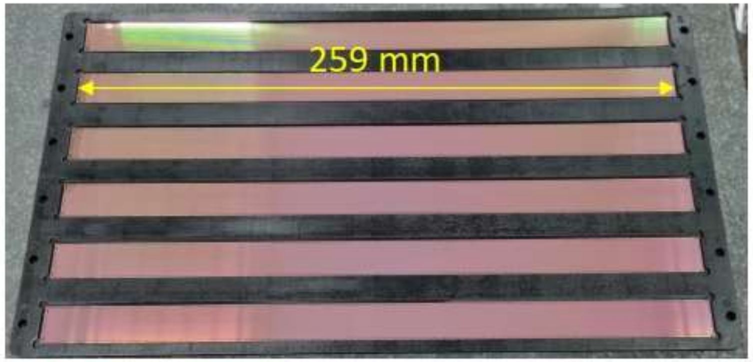


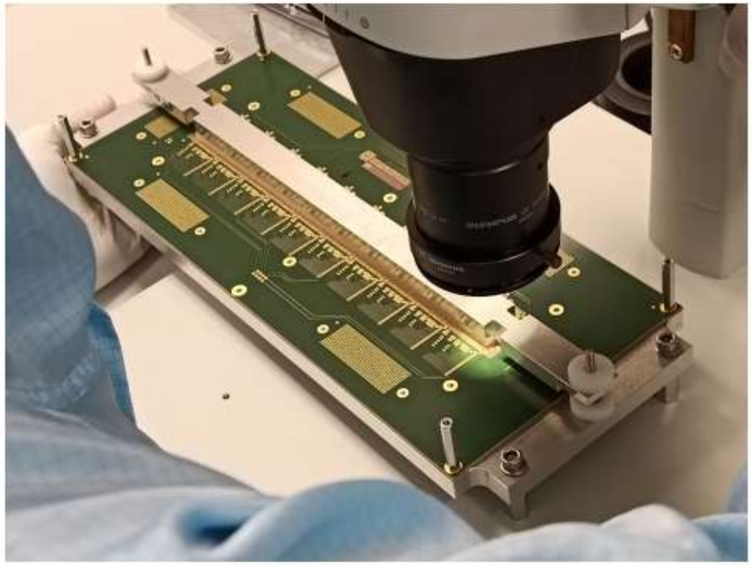
ER1 postprocessing

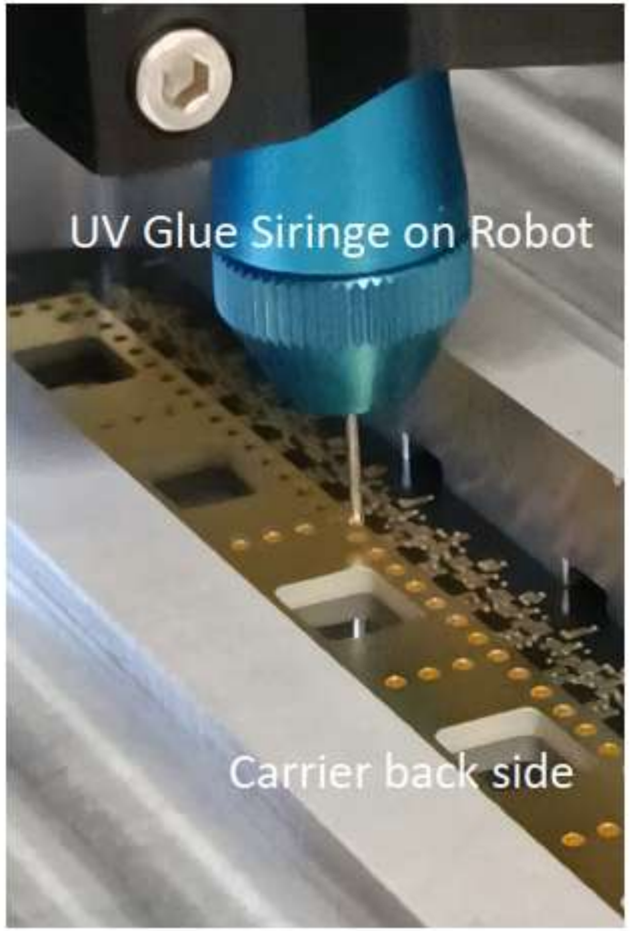
Pick, align, glue MOSS on Carrier







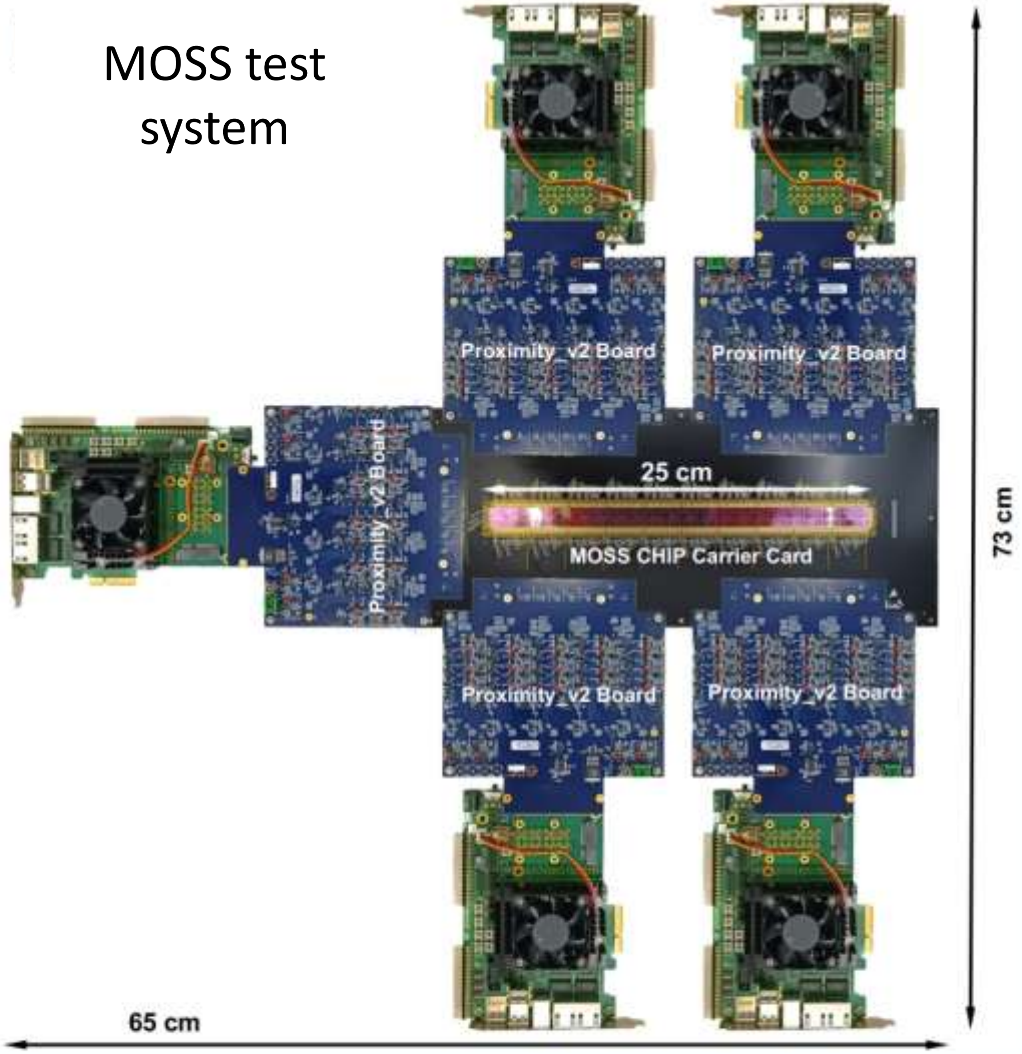


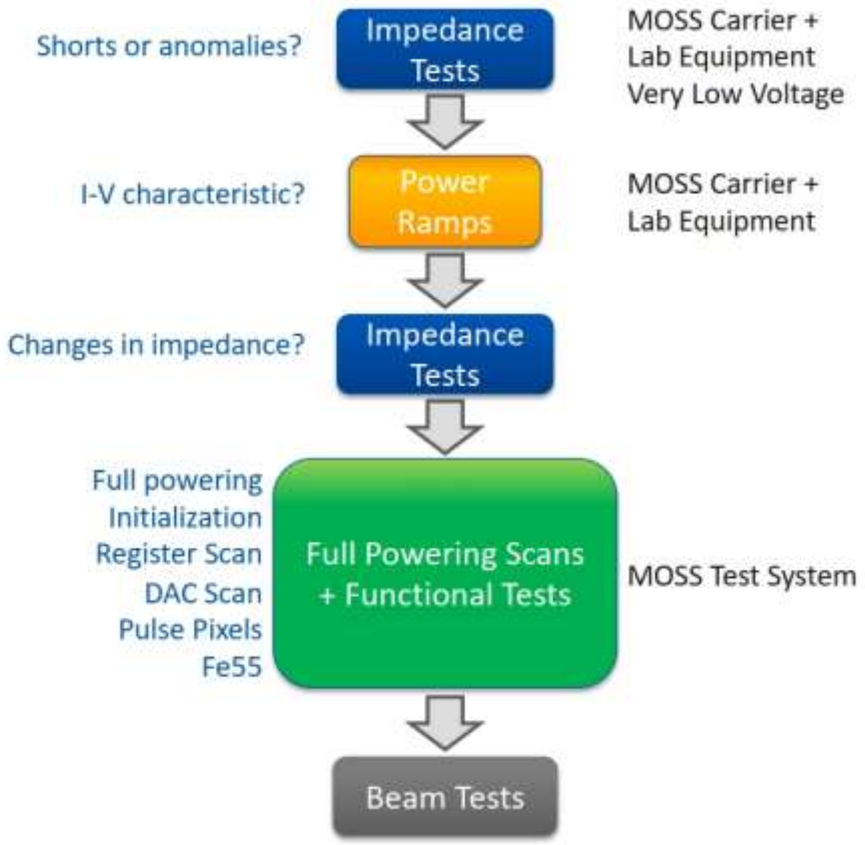


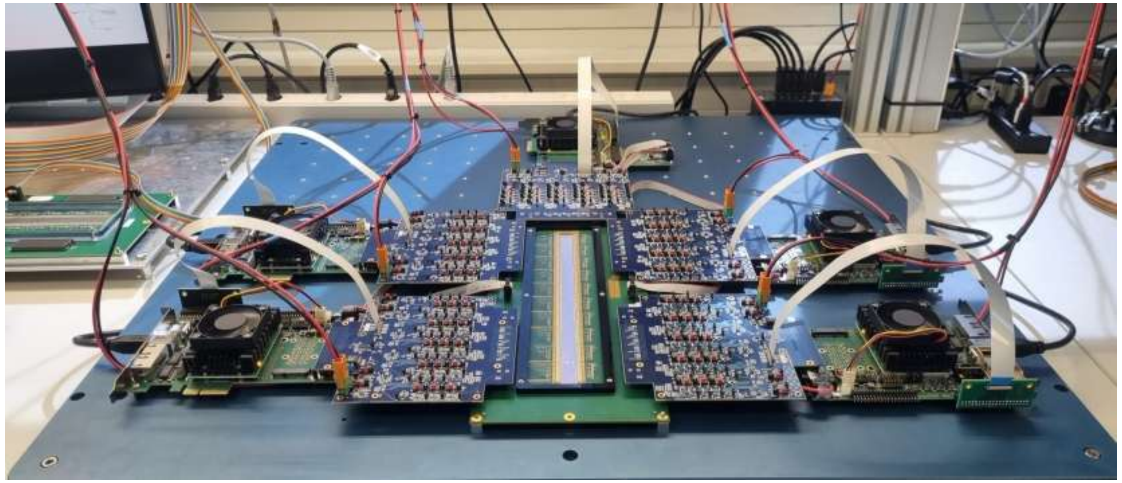
MOSS wafer handling

How to test such large sensor?

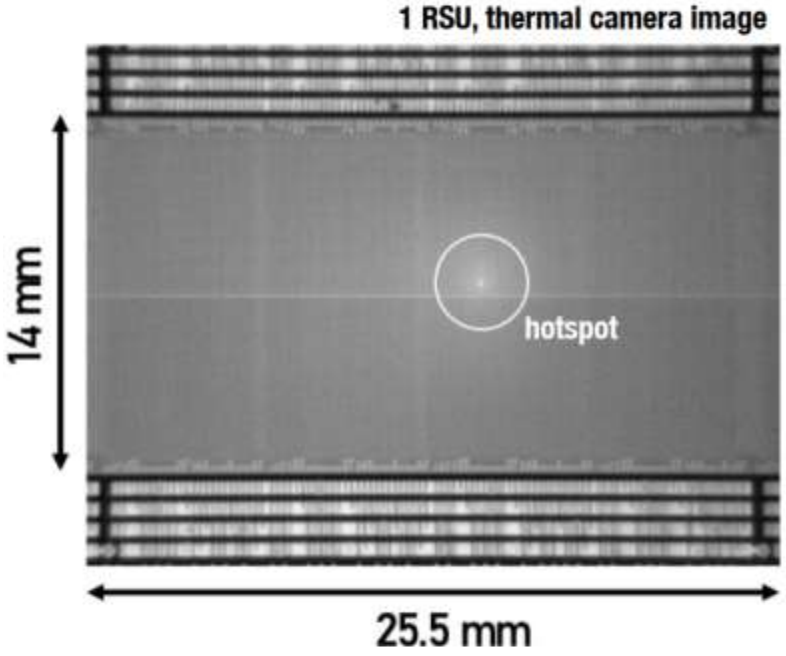
MOSS test system



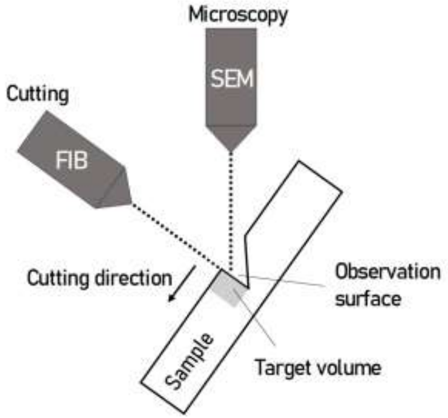




MOSS yield – powering

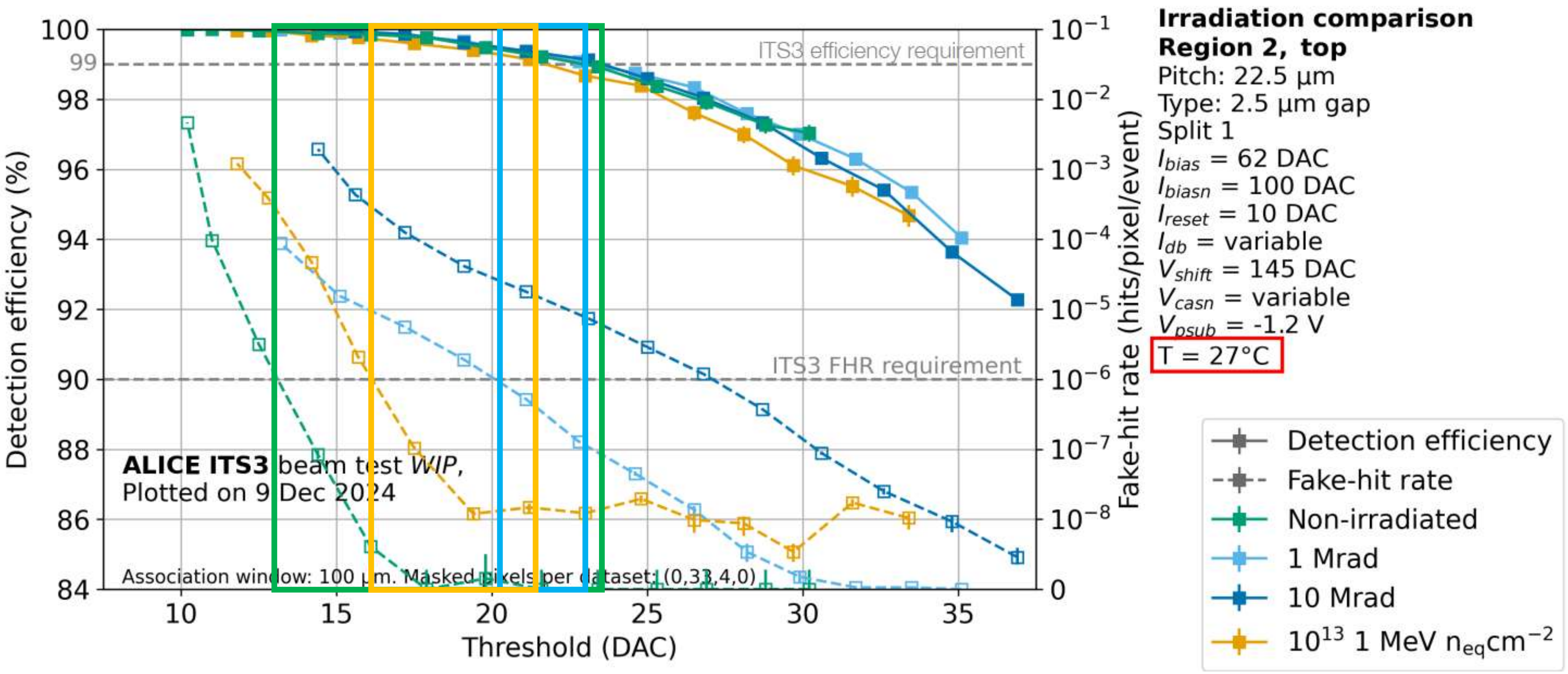


SEM (Scanning Electron Microscopy) cross section of the top two metal layers



- Power ramps were conducted while monitoring with a thermal camera
  - Hotspots were observed in chips exhibiting shorts
- A relatively large number of shorts are observed
- Reason identified (shorts between metal layers)
  - This issue was reported to the foundry, which expressed strong interest and later confirmed similar issues in other products
- Metal stack change foreseen to facilitate power distribution → expected to mitigate/resolve this issue

MOSS test beams



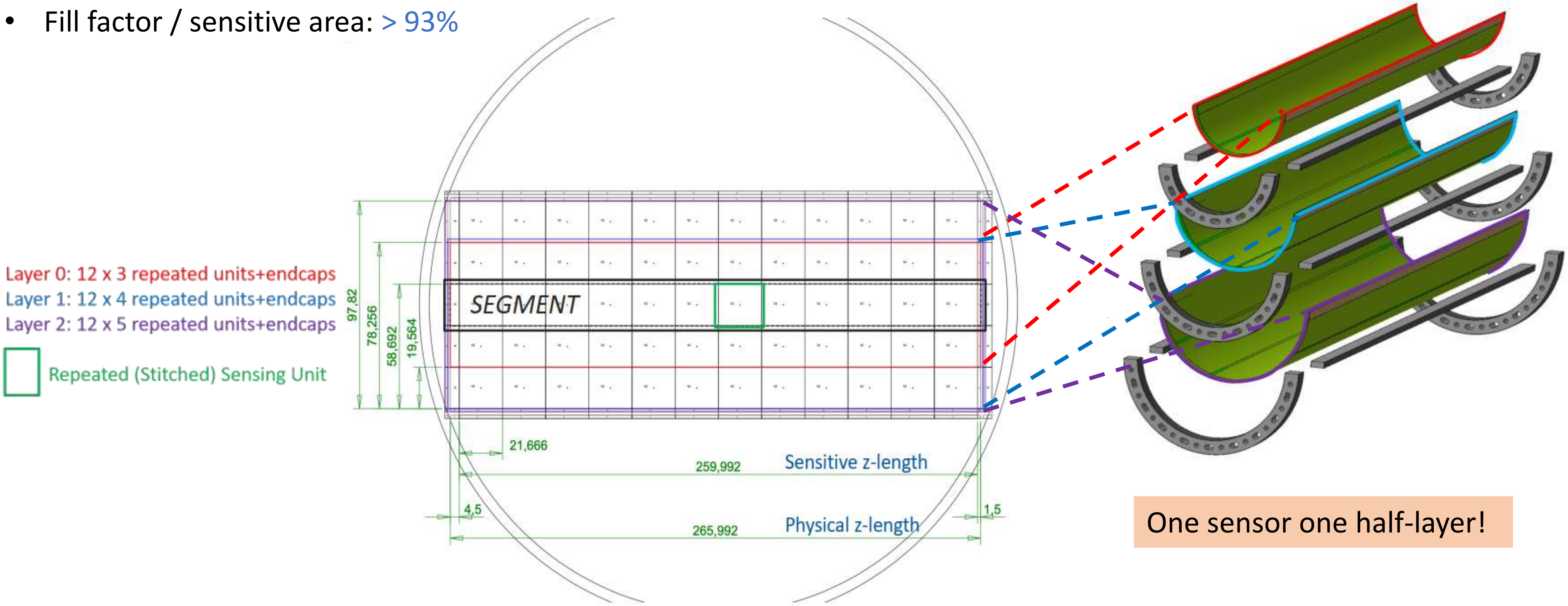
- Good operational margin before irradiations → confirmed performance from previous submissions
- Operational margin is maintained at ALICE radiation levels

Stitching works!

The final sensor prototype

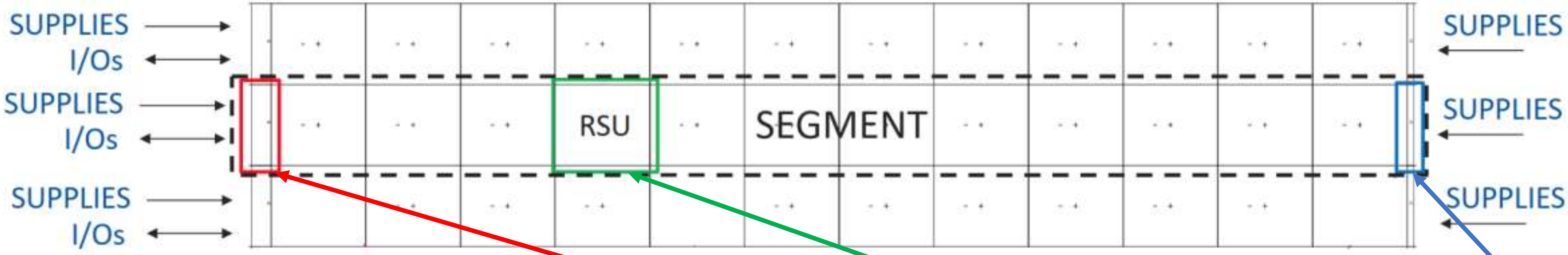
Final full size, full functionality sensor - MOSAIX

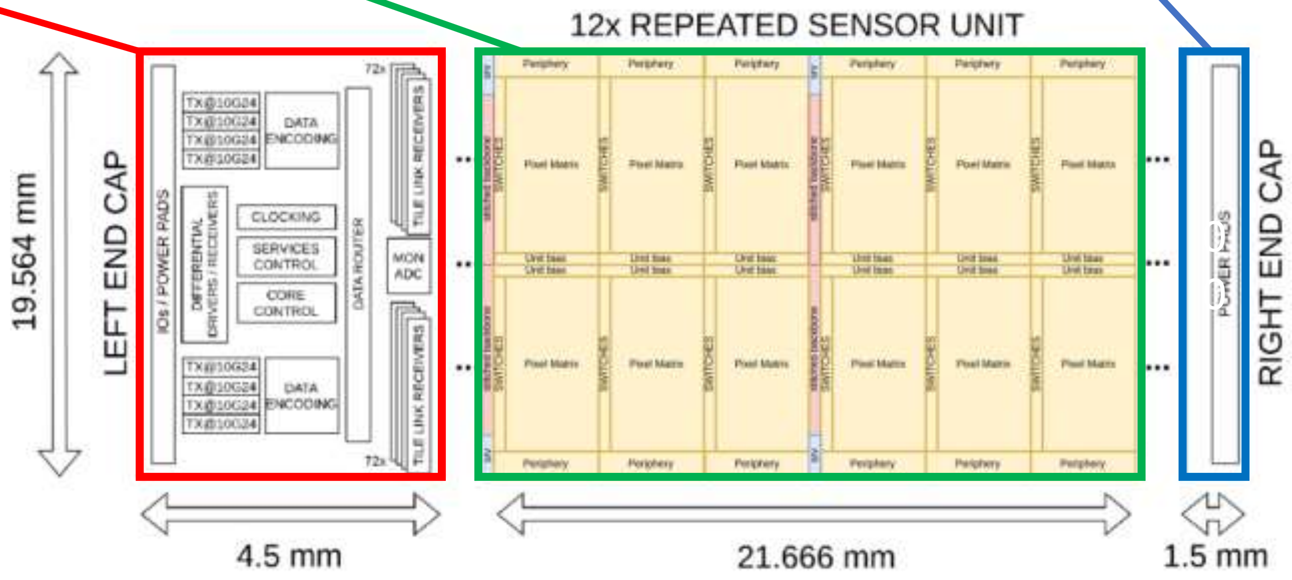
- Modular design
  - Sensor divided into 5 segments (allowing to use 3, 4 or 5 segments for layers 0, 1 and 2, respectively)
- Fill factor / sensitive area: > 93%



One sensor one half-layer!

MOSAIX

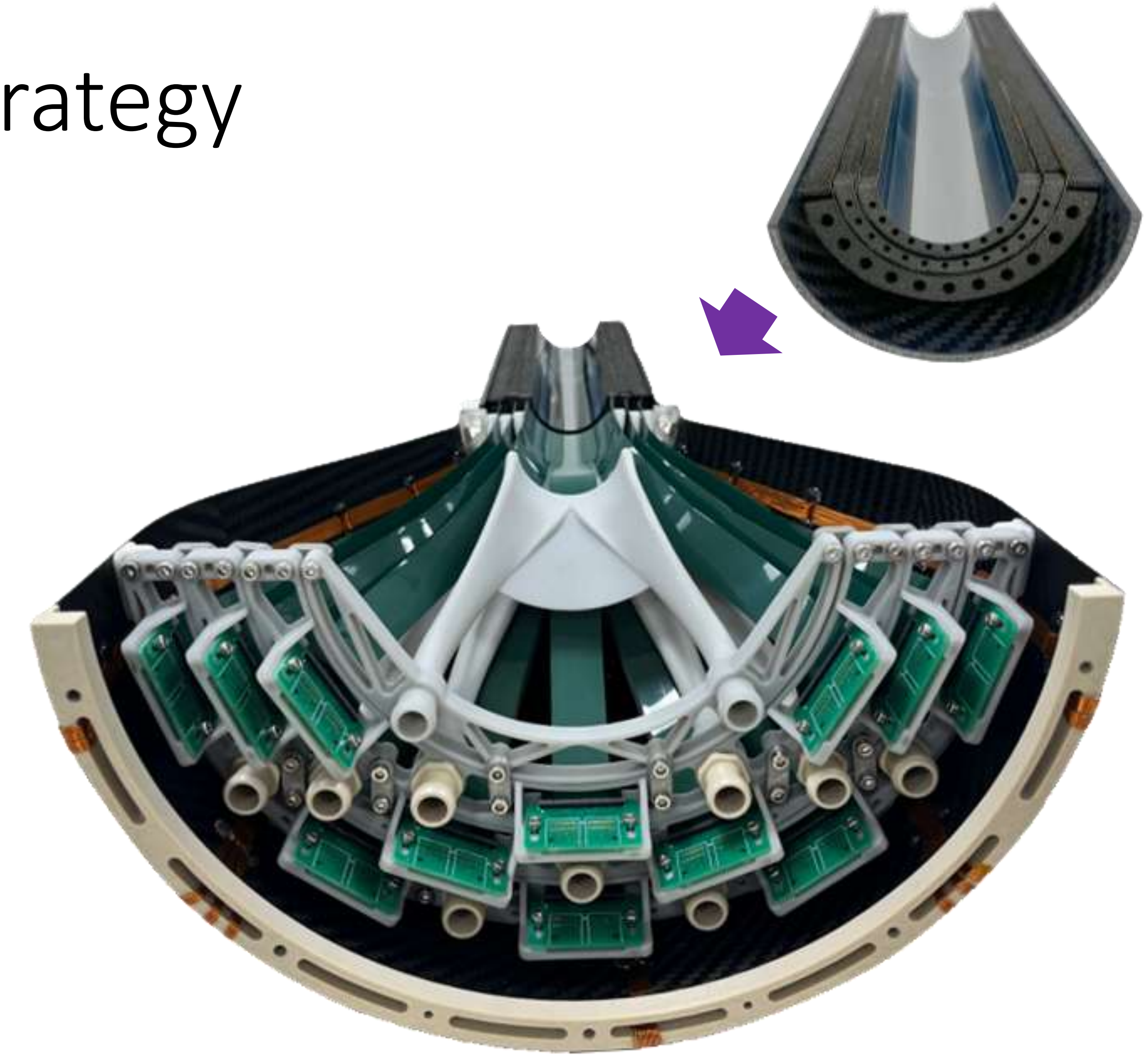




- Interfacing from the Left End Cap (LEC) and Right End Cap (REC)
  - Powering from both sides
  - Control and readout from the LEC only
  - LEC is equivalent to 8 lpGBTs
- 12 RSU per segment, 12 TILEs per RSU
- 144 TILEs can be switched on, biased and read out independently
- Power consumption: 40 mW/cm^2
- Yield target: > 98% of pixels active
- Submitted in July 2025

System development strategy

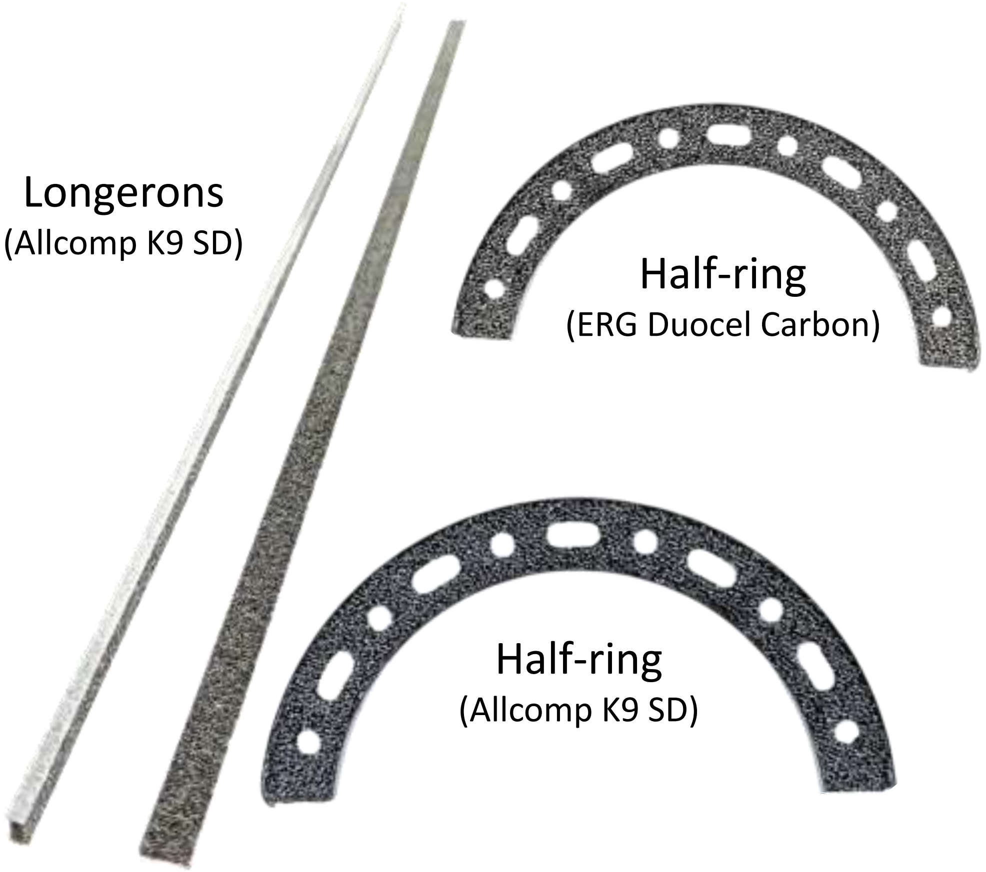
- BreadBoard Models (BBMs)
  - Initial prototypes representing selected features of the final design
- Engineering Models (EMs)
  - Used for design development; composed of a mix of final-grade and commercial components
- Qualification Models (QMs)
  - Fully integrated, final-grade assemblies including MOSAIX sensors (final full functional prototype), used for qualification tests
- Final Models (FMs)
  - Two final half-detectors for installation, plus two spare half-detectors



Full scale EM

Mechanics and cooling solutions

- Carbon foam used as support and radiator



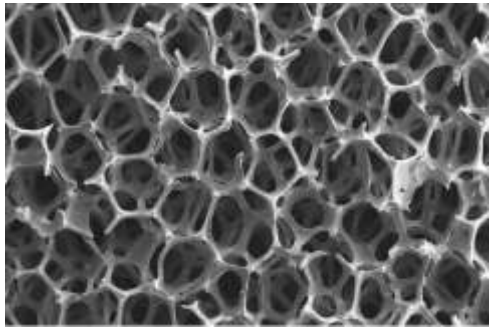
Support

ERG Carbon

@Duocel

ρ = 0.045 kg/dm^3

k = 0.033 W/m·K



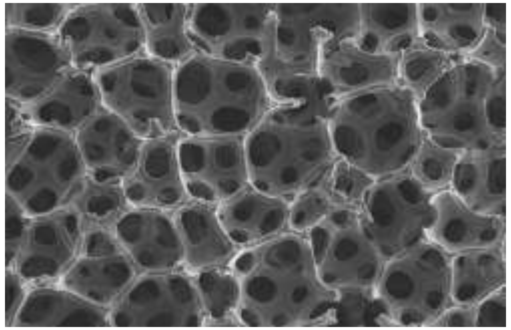
Support & **cooling**

K9

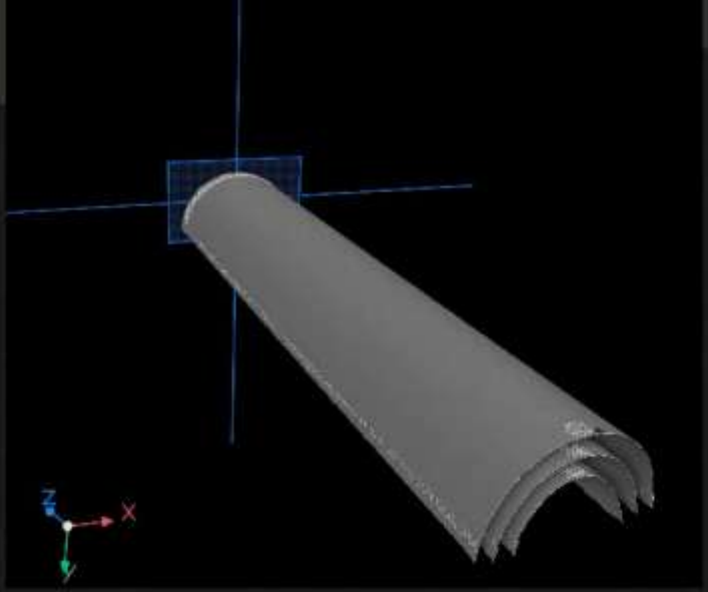
Standard Density

ρ = 0.2-0.26 kg/dm3

k = >17 W/m·K

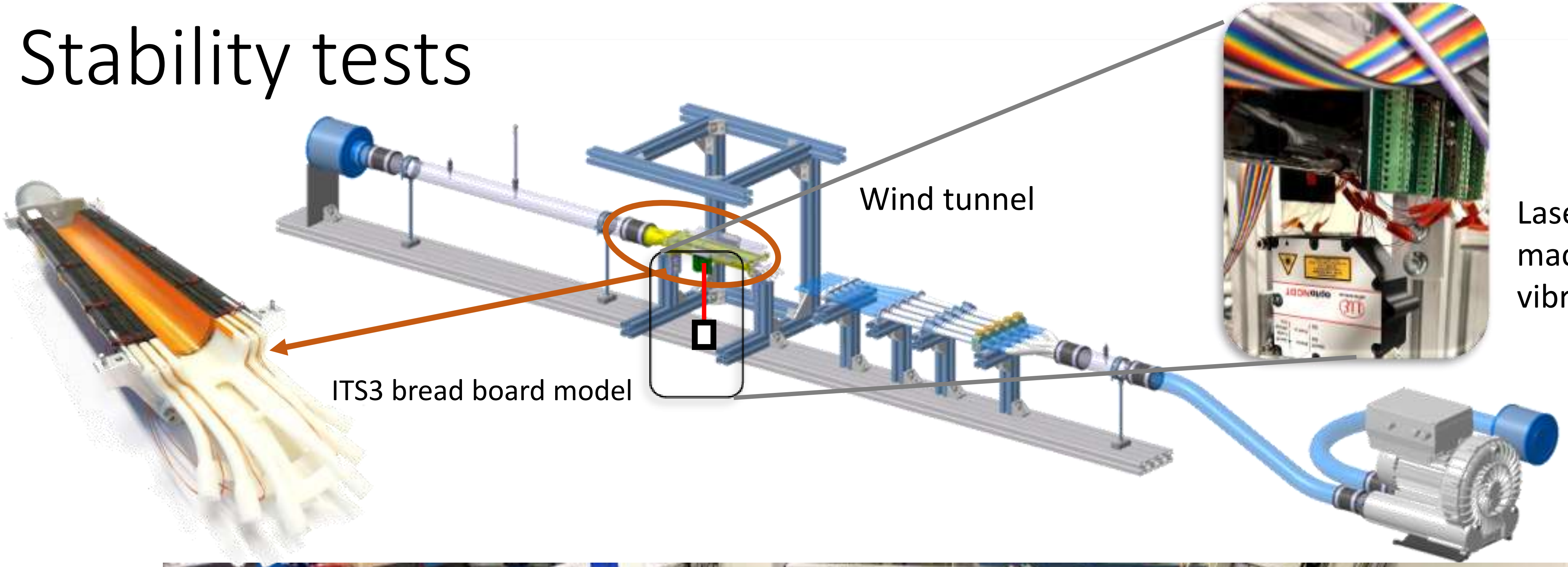


X-ray tomography

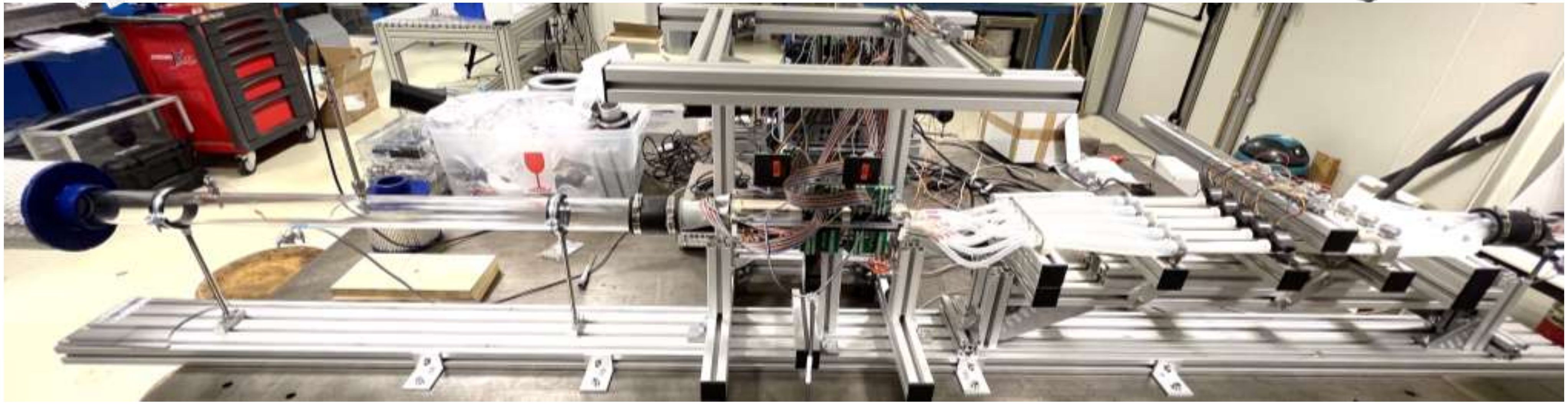


- Assembly procedure developed
- Gluing optimised

Stability tests



Laser measurement machine for vibration analysis

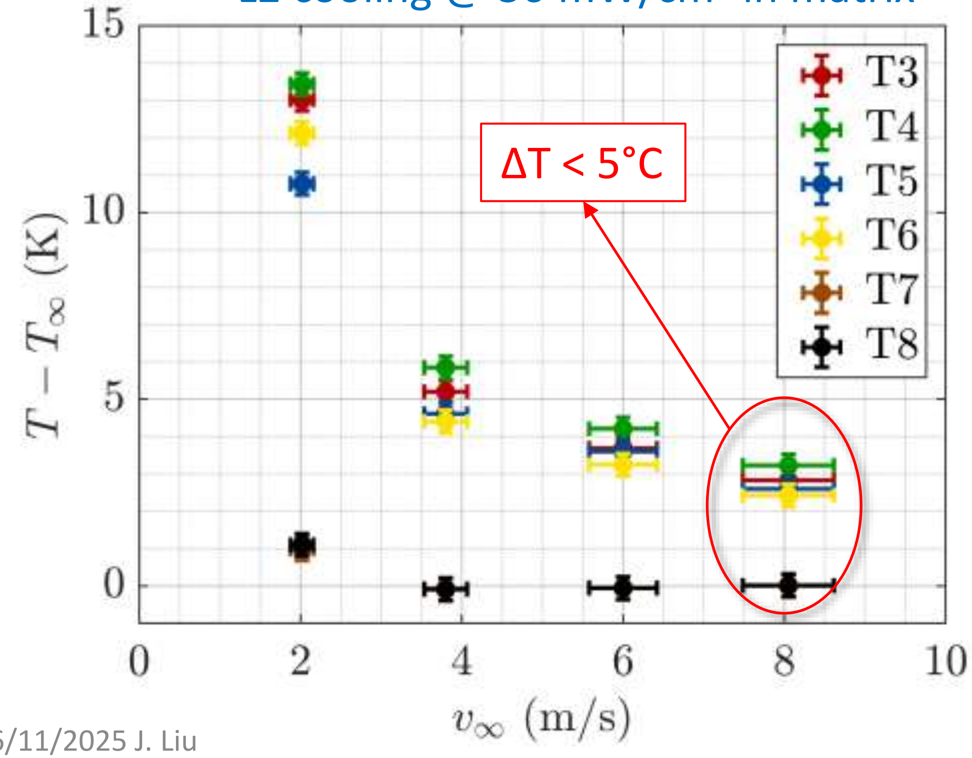


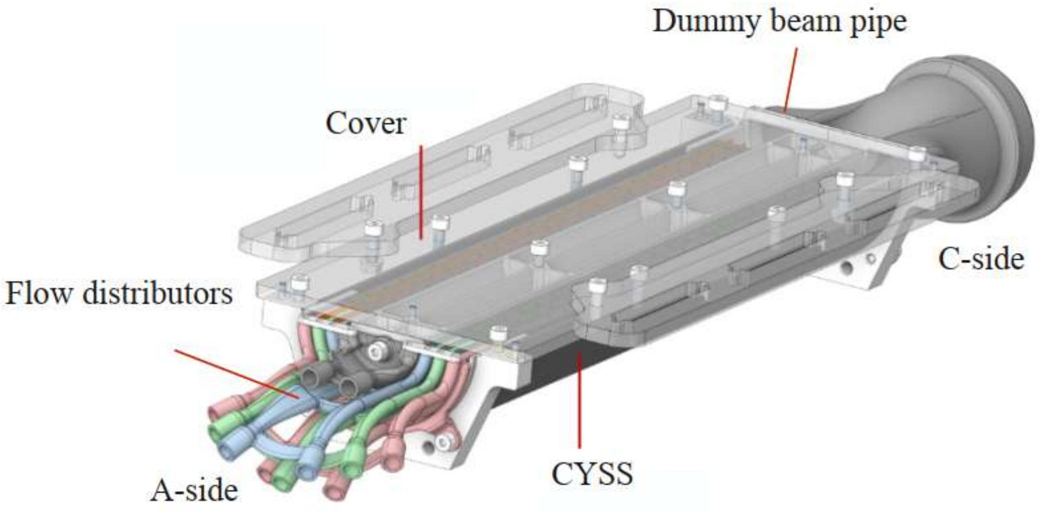
Air cooling analysis

Thermal characterization setup

- Dummy silicon equipped with copper serpentine simulating heat dissipation in matrix (50 mW/cm^2) and end-cap (1000 mW/cm^2) regions
- 8 PT100 temperature sensors distributed over the surface of each half-layer

L2 cooling @ 50 mW/cm^2 in matrix



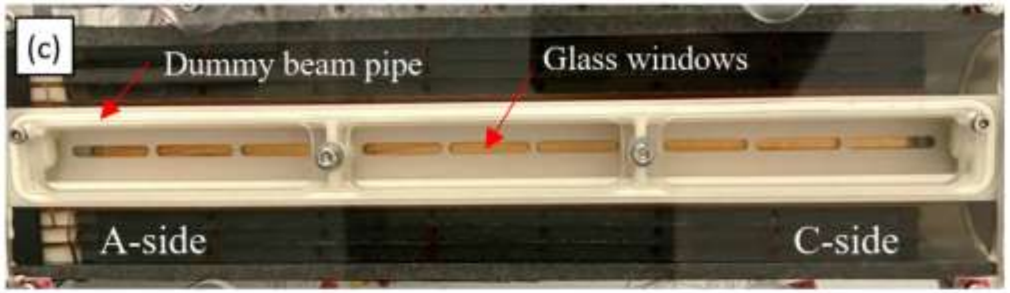


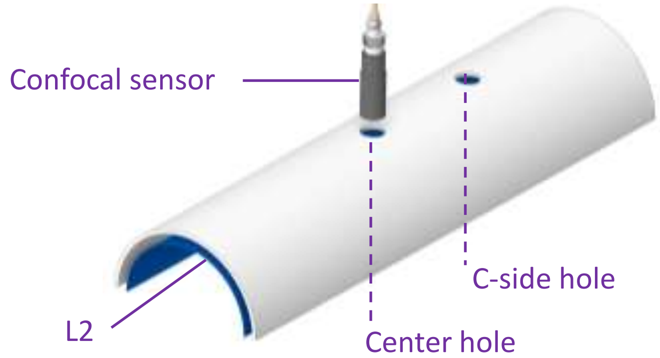
Temperature sensor position and nomenclature

- Temperature inlet air (T_∞) = 20°C,
- The detector can be operated at a temperature of 5 degrees above the inlet air temperature

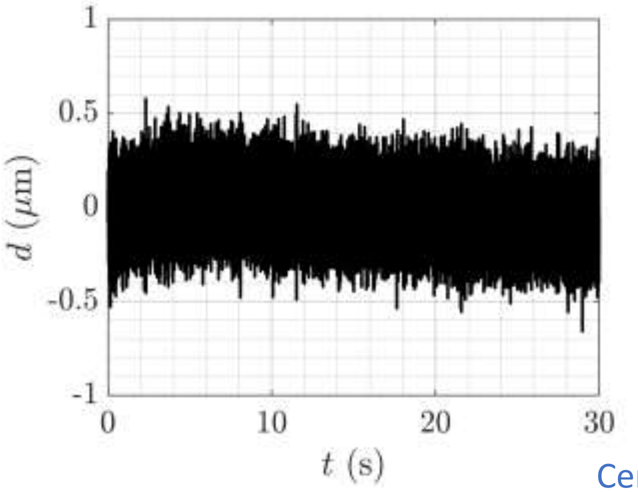
Vibrational study

- Non-contact displacement sensors for vibration measurements → avoid perturbation of the airflow approaching the half-layers
- Glass windows implemented on the dummy beampipe and CYSS → allow displacements on the half-layer 0 and 2 to be measured

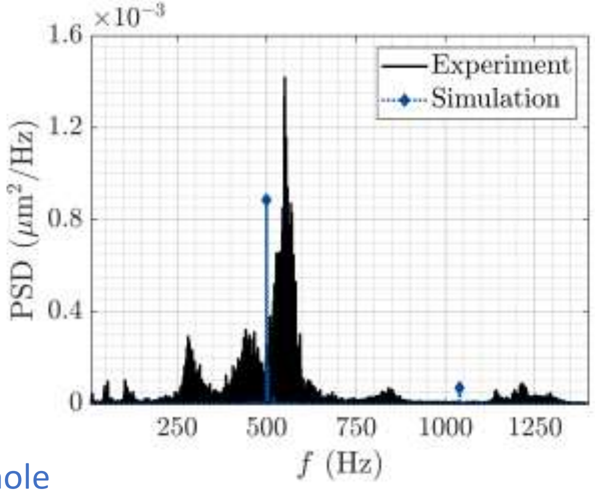




Displacement vs. time



Power spectral density of the displacements



Center hole

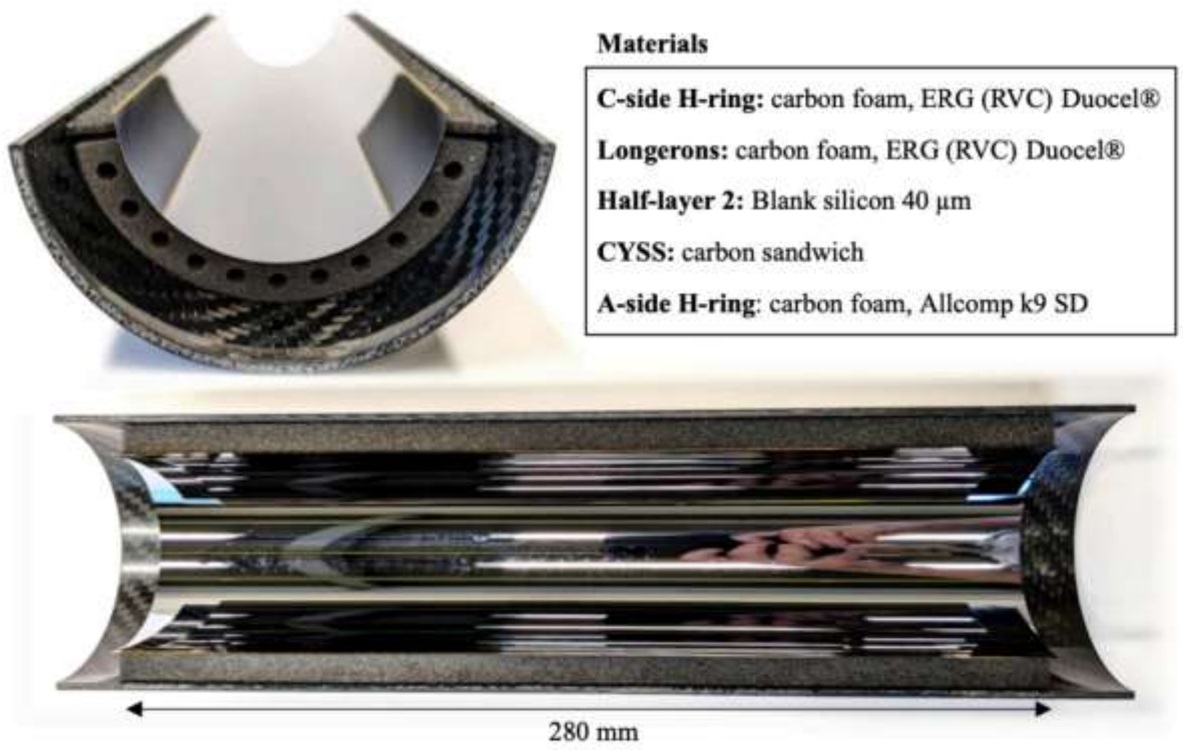
half-layer 2, v_∞ = 8 m/s

- Peak-to-peak ~ 1.1 μm
- rms of the displacement < 0.4 μm

Thermoelastic tests

Thermoelastic expansion setup

- Differential thermoplastic expansion caused by short-term temperature fluctuation among different components could introduce failures
- Final grade material half-layer assembly in climate chamber (up to 40 °C by steps of 2 °C)

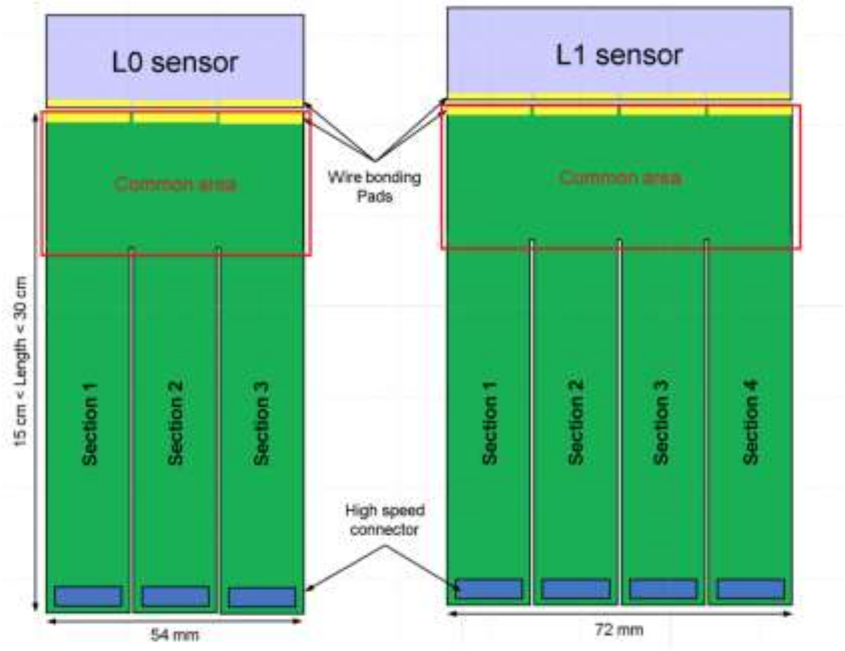


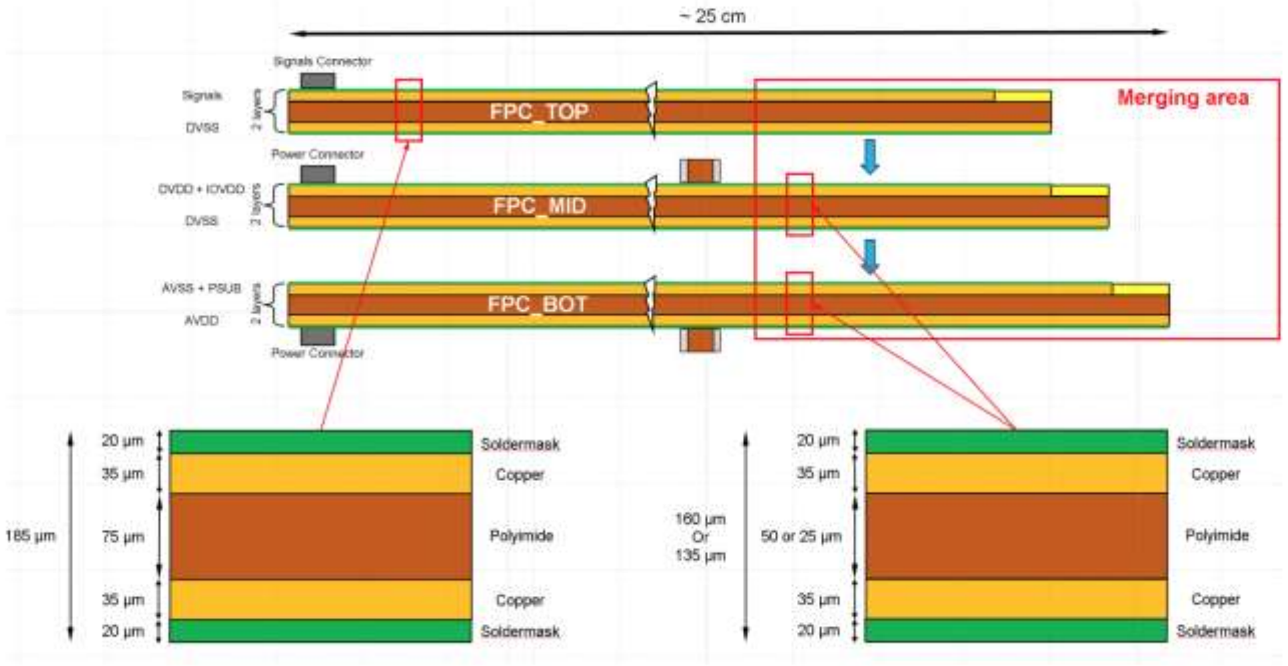
- Several thermal cycles for a total of 50 hours → assembly unaffected
- Further tests will be performed to investigate rapid increase of the temperature and maximum failure temperature

Interconnection (1/2)

Flexible printed circuits (FPC) for communication and powering

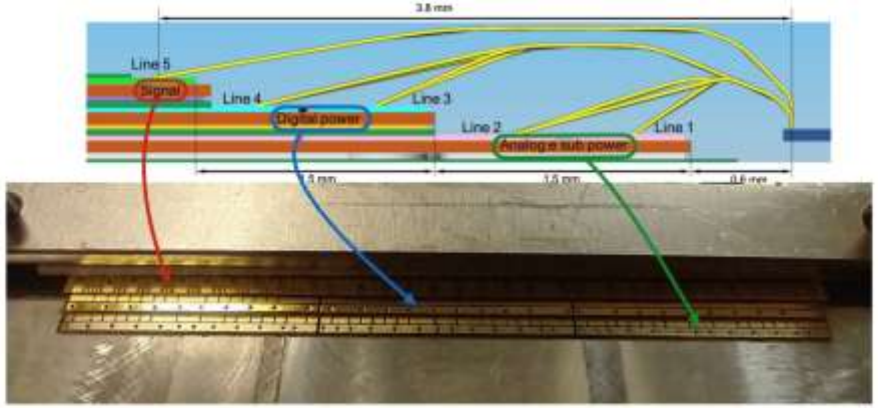
- Placed outside the sensible area
- 3,4 or 5 sections corresponding to the number of detector chip segments of the half-layer
- Three double copper layers flex, multi-strip shaped (15-30 cm long), connected in a concentrated merging area

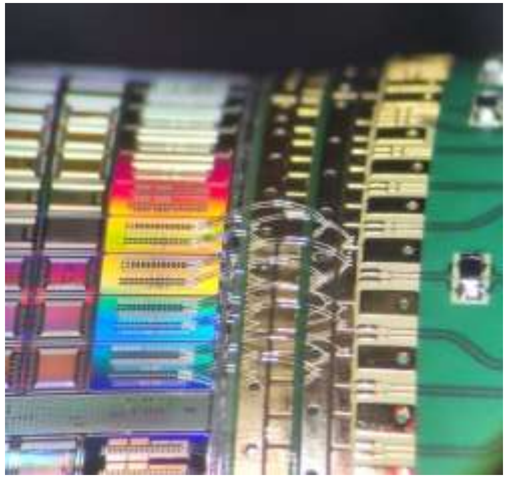




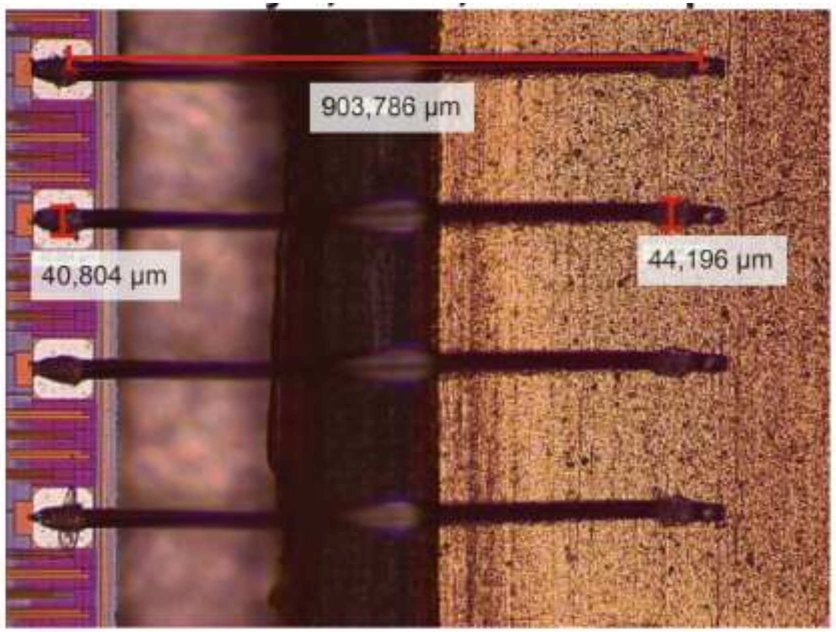
Interconnection (1/2)

- Interconnection through wire-bonding at the edge of the sensor verified
- Wire-bonds loops optimized based on pull-force measurements with ALPIDE sensors

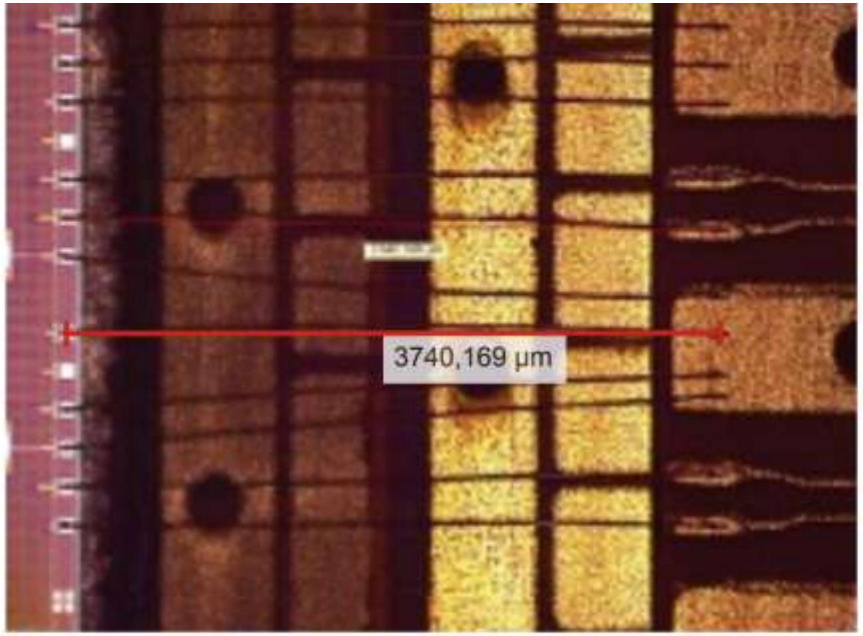




Wire-bonding to MLR1 prototypes

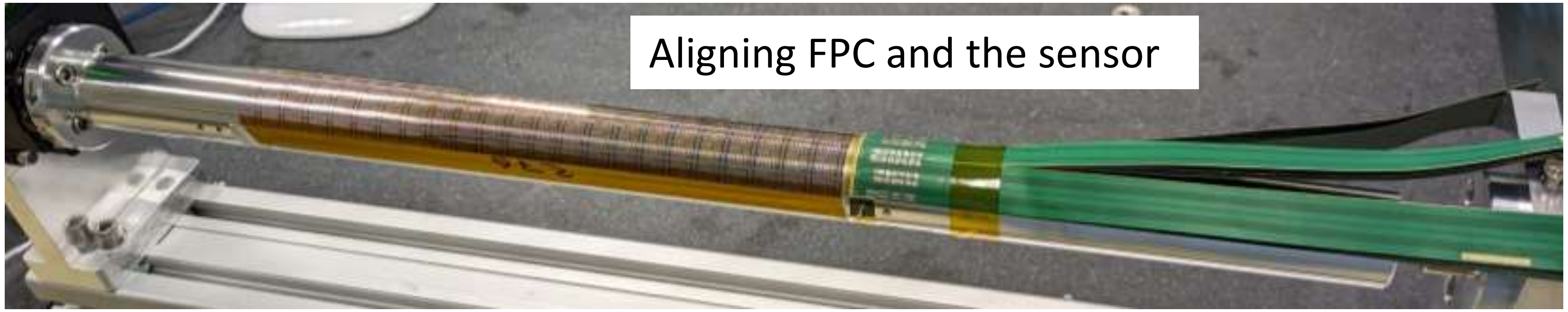


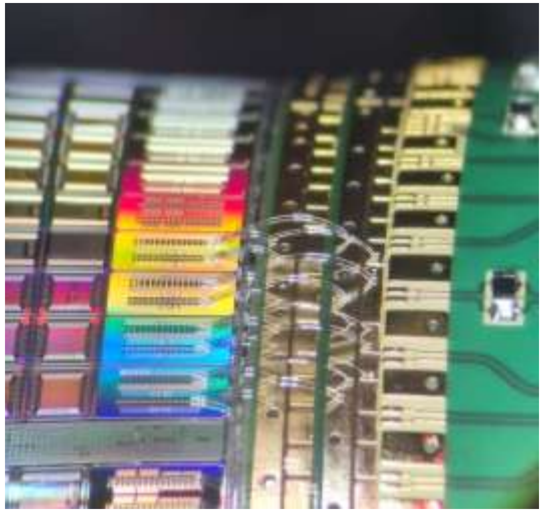
Bottom layer, line 1



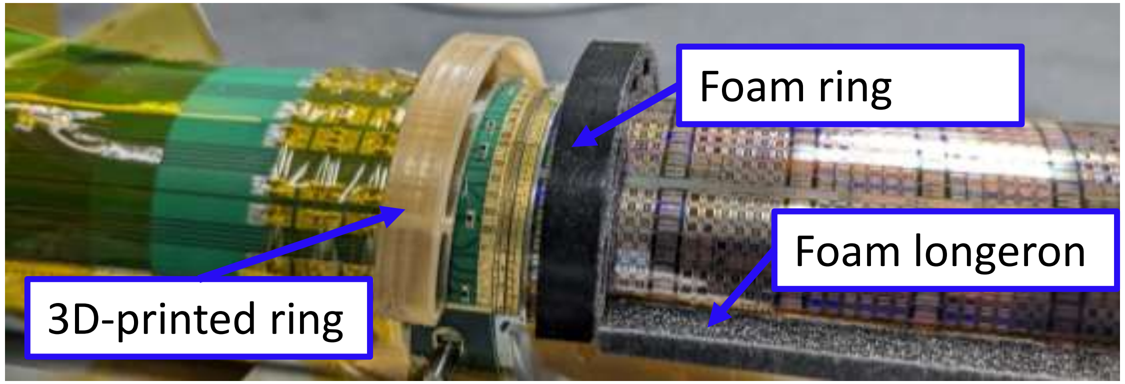
Upper layer, line 5

Assembly practicing





Wire-bonding for the curved sensor

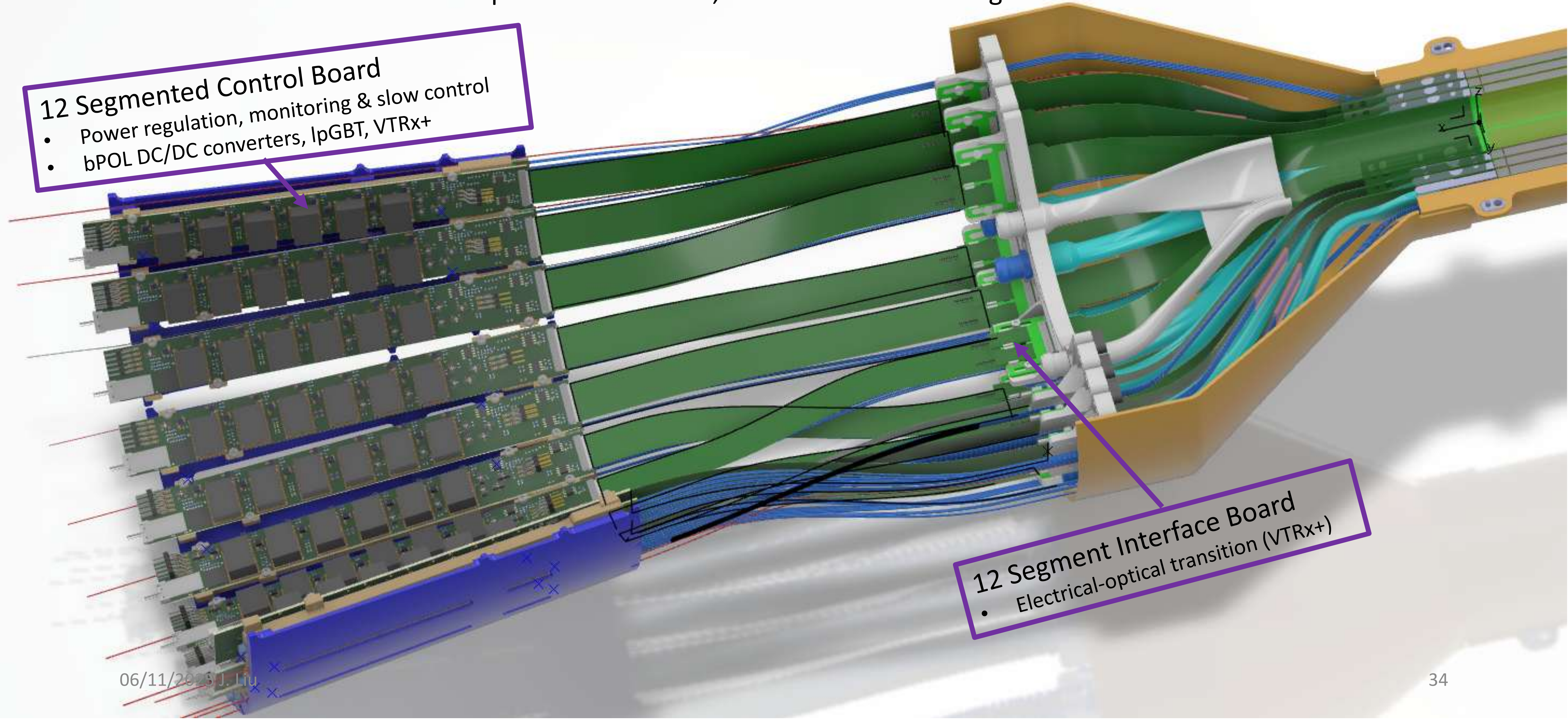


Gluing of foams and additional supports

Assembled first prototype layer of ITS3

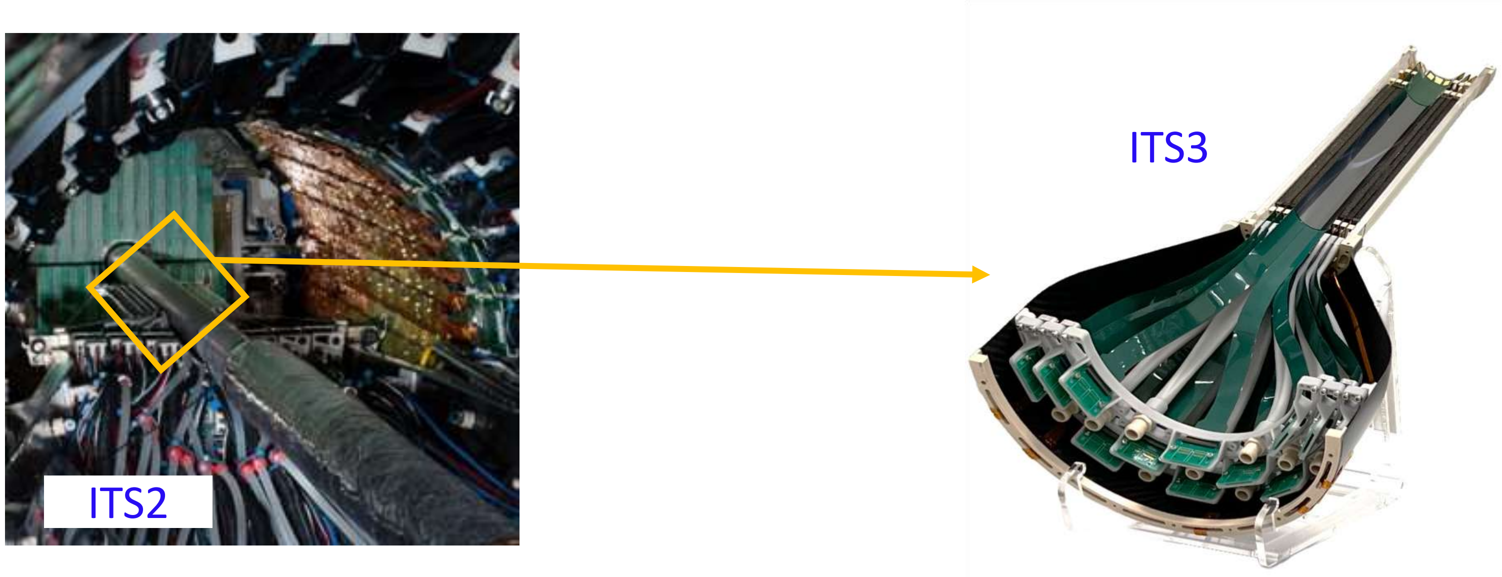
Detector Service Electronics

- 1 Detector Power Board for central power distribution, control and monitoring



ITS3: Key achievements and impact

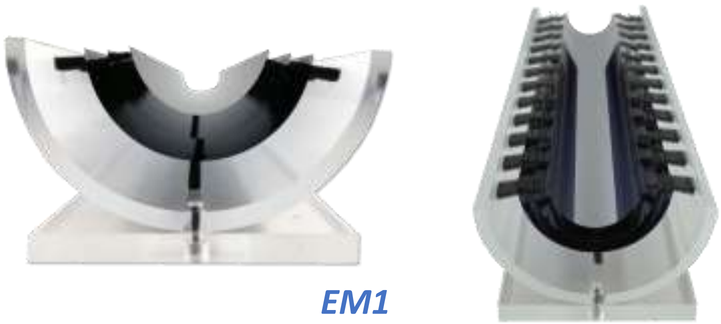
- ITS3: replaces inner ITS2 layers with wafer-scale, curved 65 nm CMOS sensors, achieving
- Physics impact: improved vertexing precision and reduced backgrounds for heavy-flavour and low-mass dielectron measurements
- Innovation: first truly cylindrical tracker with wafer scale stitched sensors
- Broader reach: enabling technology for EIC, CEPC,, FCC-ee, etc
- Status: design specifics finalized; large-area prototypes in fabrication; installation foreseen for LS3 (2026–2030)



Backup

Mechanical prototypes

- Engineering models (EMs): used for design development, a mixture of final-grade components and commercial components

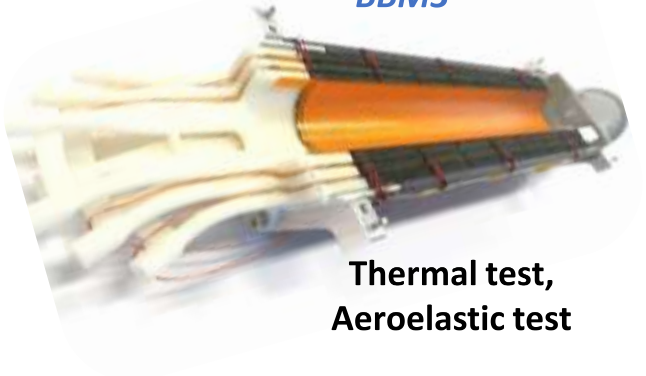


EM1

EM2

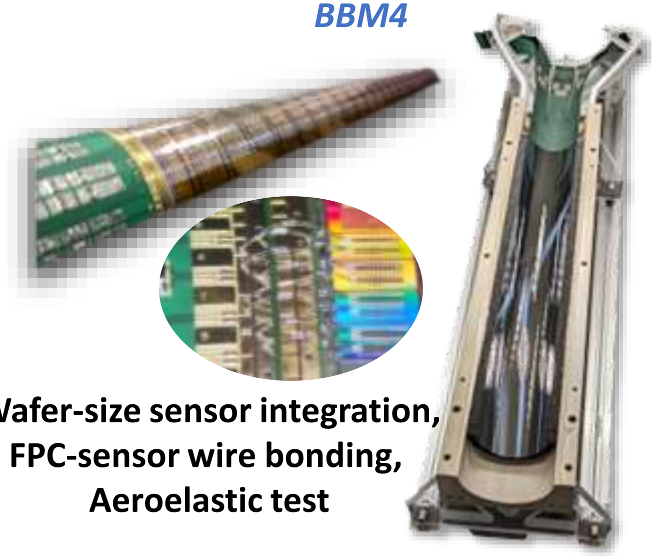
- Breadboard models (BBMs): test samples and initial prototypes, partially representative of some of the final model features

BBM3



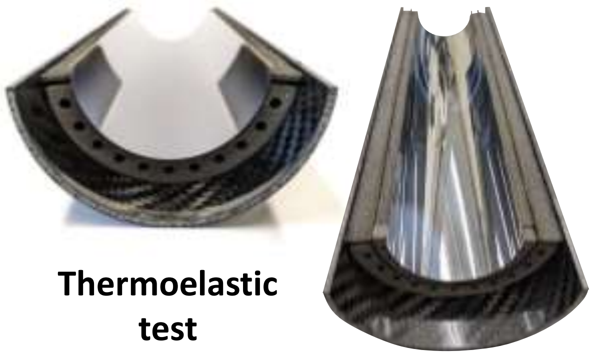
Thermal test, Aeroelastic test

BBM4



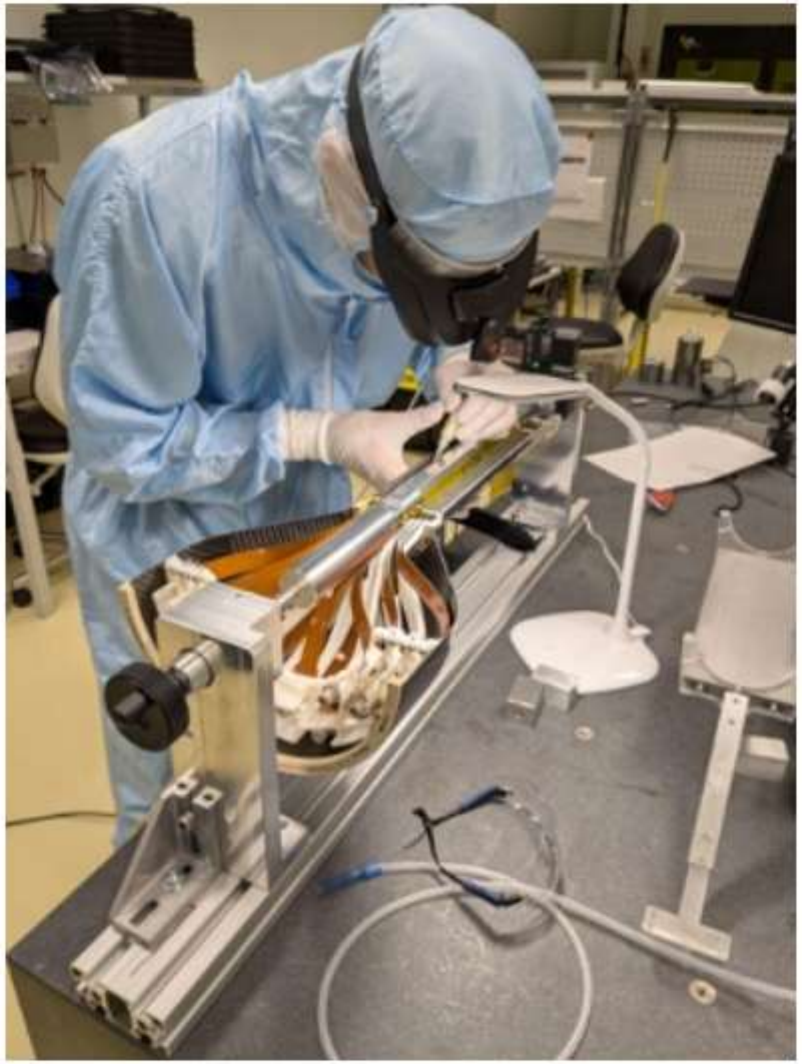
Wafer-size sensor integration, FPC-sensor wire bonding, Aeroelastic test

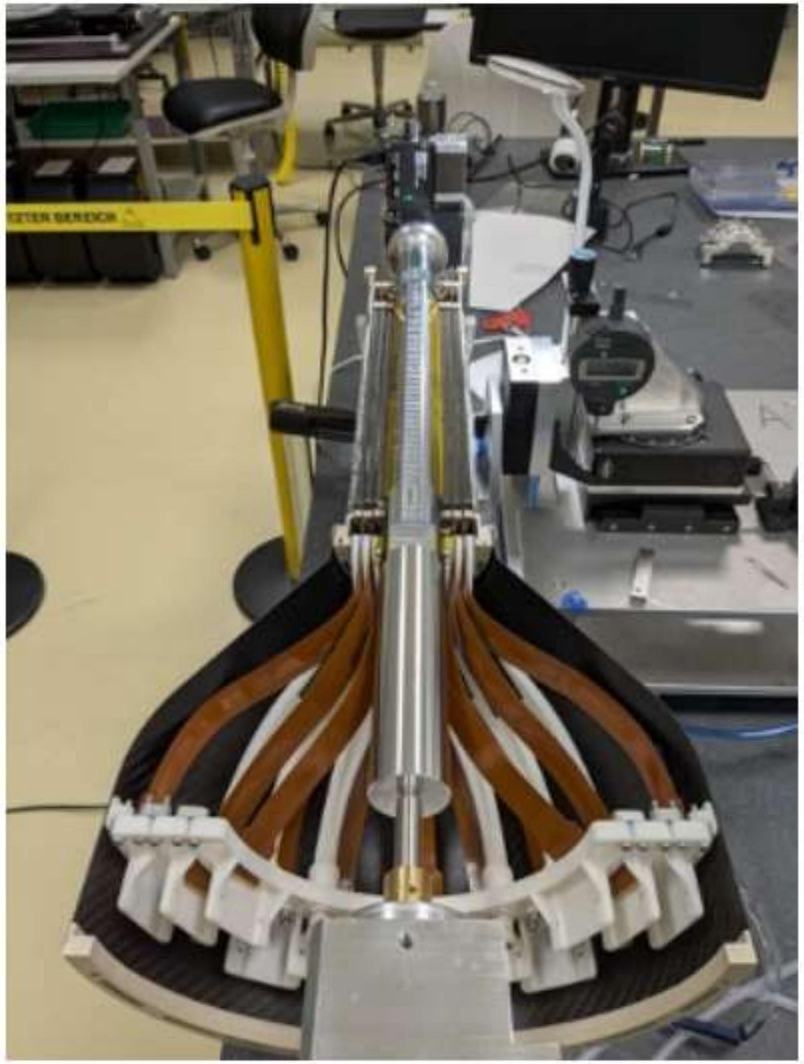
BBM5



Thermoelastic test

EM models with service



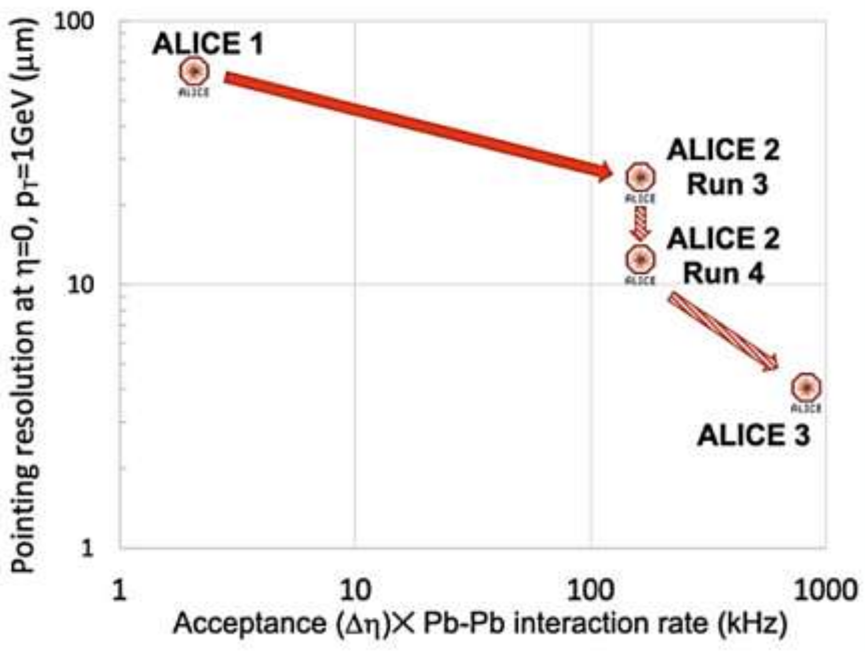


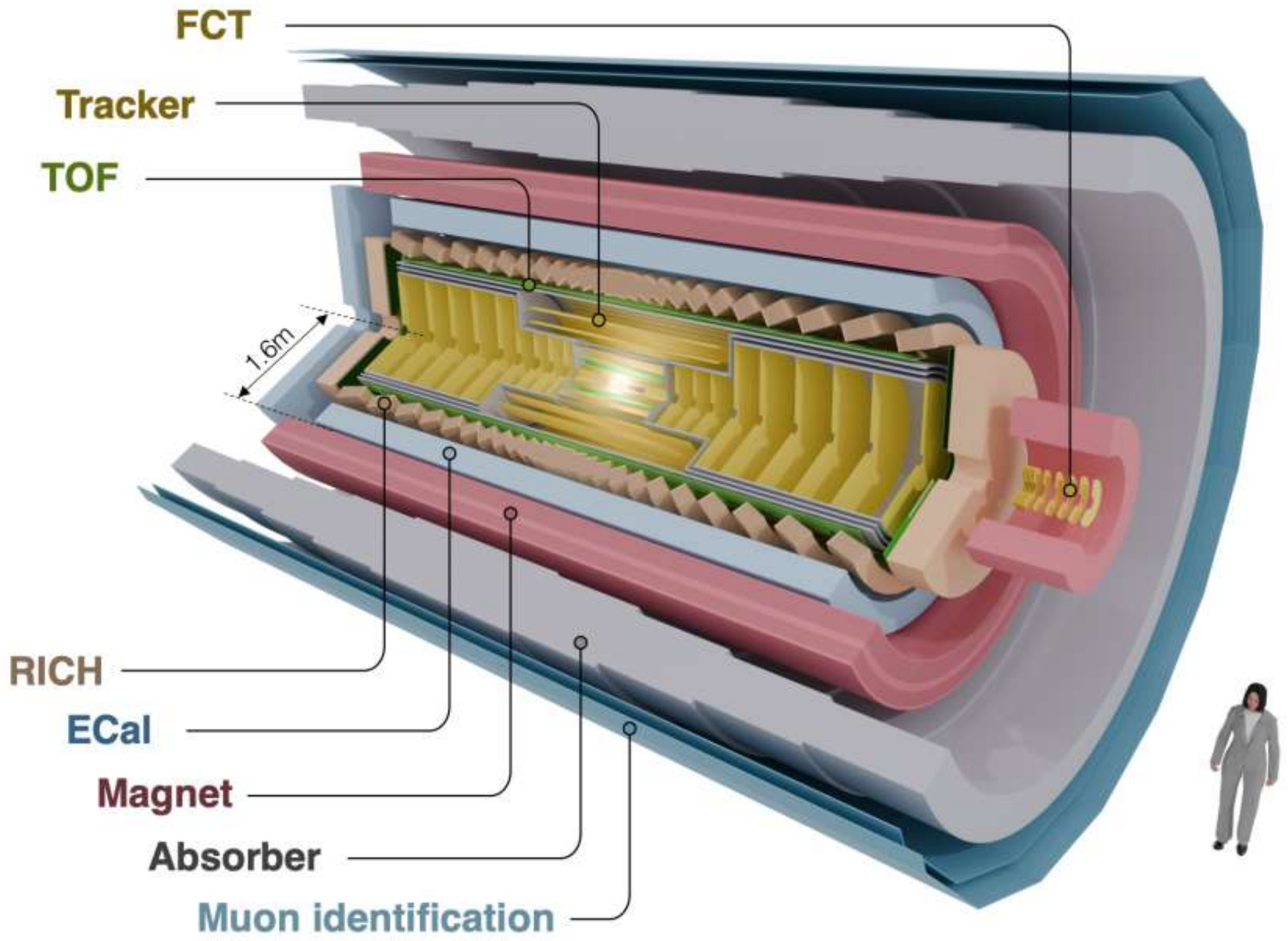
ALICE 3

ALICE 3 LoI: CERN-LHCC-2022-009

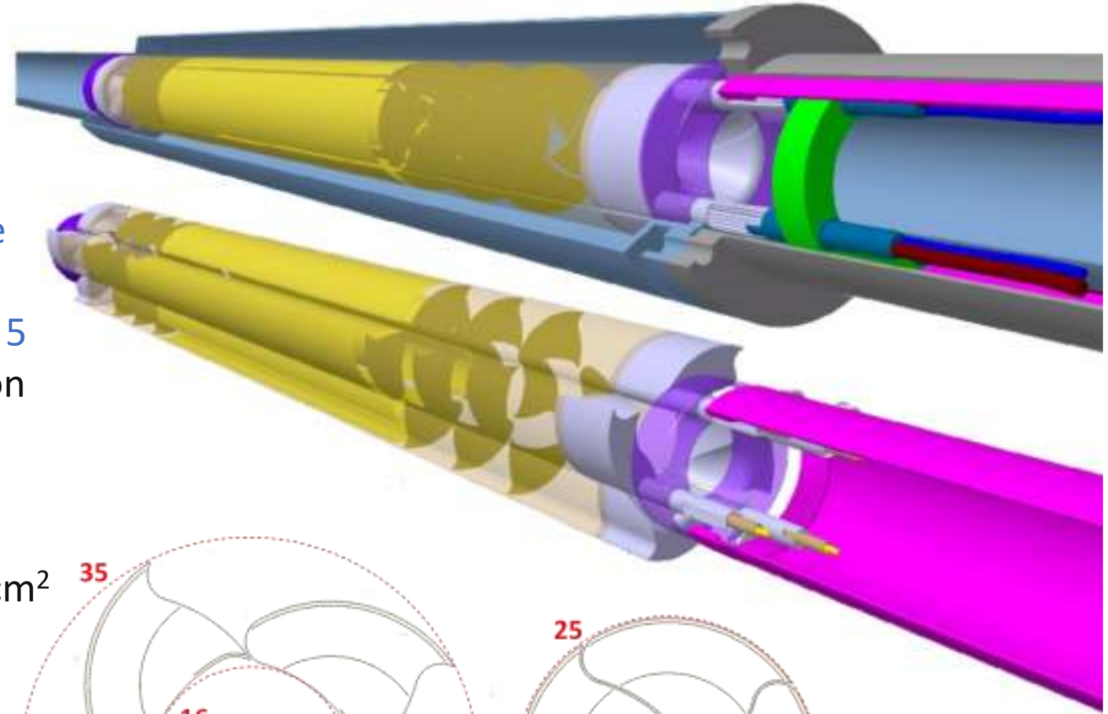
Novel and innovative detector concept

- Compact and lightweight all-silicon detector
- Retractable vertex detector
- Superconducting magnet system
- Continuous readout

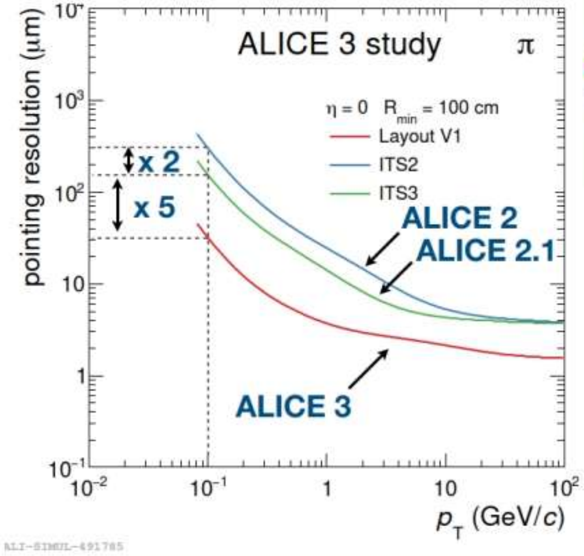


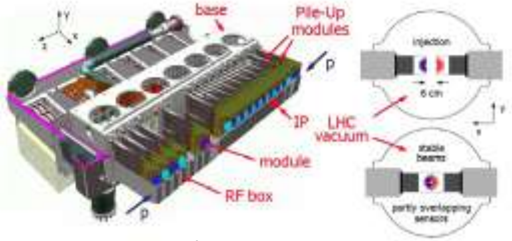


ALICE 3 - Vertex detector

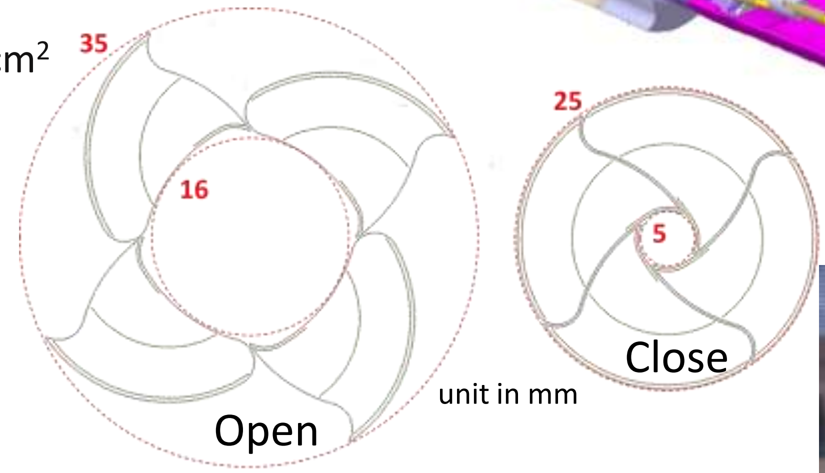


- 3 layers of wafer-size, ultra-thin, curved, CMOS MAPS inside the beam pipe in secondary vacuum
- Retractable configuration thanks to movable petals: distance of 5 mm from beam axis for data taking and 16 mm at beam injection
  - Similar concept to LHCb VELO, but in barrel configuration
- Unprecedent spatial resolution: σ_{pos} ~ 2.5 µm
- Extremely low material budget: **0.1% per layer**
- Radiation tolerance requirements: 300 Mrad + 10^{16} 1MeV n_{eq} /cm^2





LHCb VELO concept



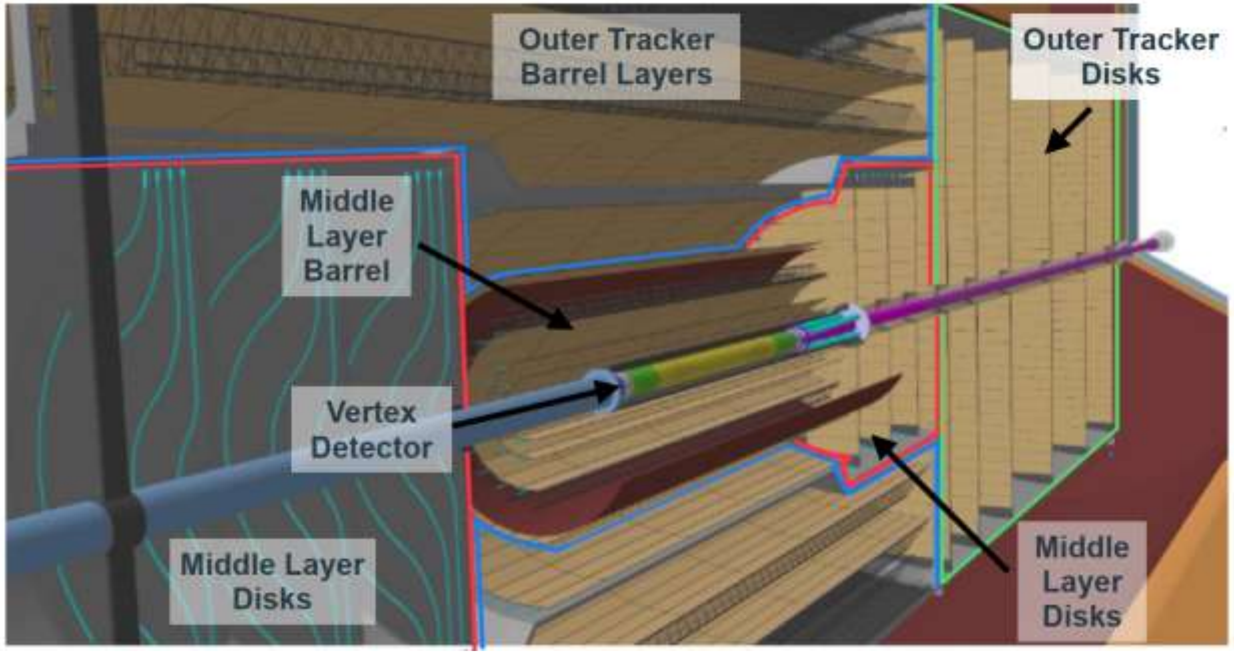
unit in mm

R&D challenges: radiation hardness, technology feature size and cooling

Bread-Board Model 3
3D-printed aluminium petals
0.5 mm wall thickness

ALICE 3 - Tracker

- Middle layers + outer tracker
  - 8 + 2 x 9 tracking layers (barrel + disks)
- **60 m² silicon pixel detector based on CMOS MAPS technology**
  - Largely leverages ITS2 and ITS3 experience
- Compact: r_{out} ~80 cm, z_{out} ± 3.5 m
- Large coverage: ± 4 η
- Time resolution: ~100 ns
- Sensor pixel pitch of ~50 µm for σ_{POS}= 10 µm
- Low power consumption: ~ 20 mW/cm²
- Low material budget: ~1% X_0 per layer



R&D challenges: module integration, high yield industrial mass production, low power consumption while maintaining timing performance and power distribution