Integration of Freestanding High-*k* Oxide Membranes for 2D Ferroelectric Field-Effect Transistors

Zejing Guo[1,2], Xuyang Sha[1,2], Fang Xu[3], Guangyi Huang[4], Changlin Zheng[4], Lingfei Wang[3], Hangwen Guo[1,2,5*], Jian Shen[1,2,4,5*] , and Wu Shi[1,2*]

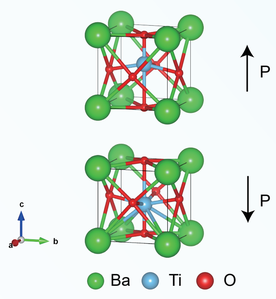
[1]State Key Laboratory of Surface Physics and Institute for Nanoelectronic Devices and Quantum Computing, Fudan University, Shanghai 200433, China [2]Zhangjiang Fudan International Innovation Center, Fudan University, Shanghai 201210, China [3]Hefei National Research Center for Physical Sciences at Microscale, University of Science and Technology of China, Hefei 230026,China [4]State Key Laboratory of Surface Physics and Department of Physics, Fudan University, Shanghai 200433, China [5]Hefei National Laboratory, Hefei 230088, China

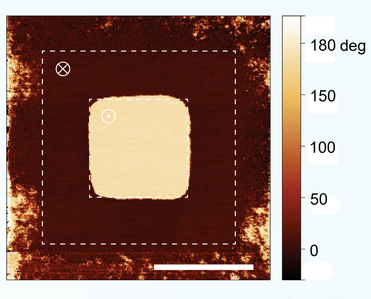
Introduction

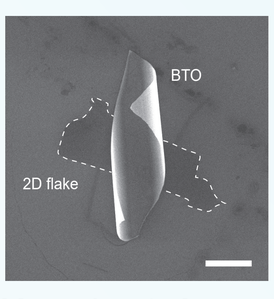
Integrating high-*k* ferroelectric oxides like $BaTiO_3$ (BTO) with 2D semiconductors offers compelling prospects for next-generation non-volatile memory and neuromorphic computing. Yet, practical implementation is hindered by substrate-induced lattice mismatch in conventional growth, as well as mechanical deformation and defect-induced leakage currents when utilizing freestanding van der Waals membranes. In this work, a defect-tolerant strategy for top-gate integration of freestanding BTO membranes with MoS_2 channels is presented. The resulting ferroelectric field-effect transistors (FeFETs) exhibit a record-high memory window of 0.22 V nm^{-1}, an ultrahigh dielectric constant of 52, and a near-ideal subthreshold swing of 60 mV dec^{-1}. Furthermore, a fully functional 3×4 top-gate FeFET array enabling in-memory logic and synaptic functionalities is demonstrated.

I. Integration of BTO with 2D Materials

Ferroelectric BTO with integration obstacles

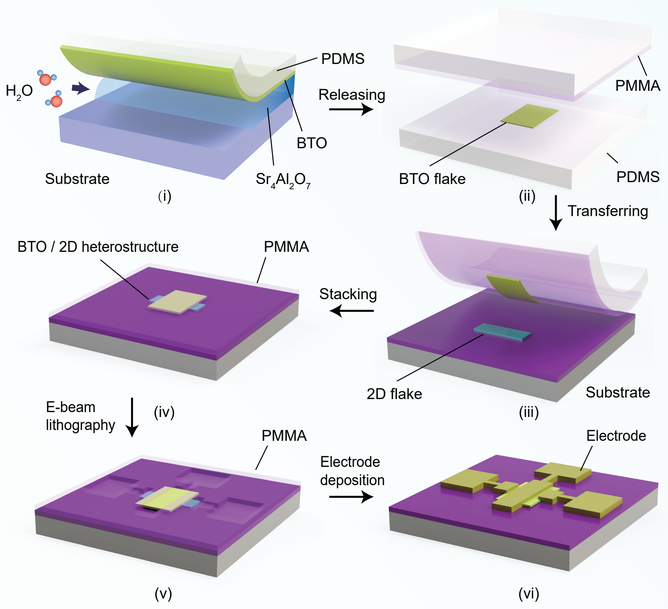


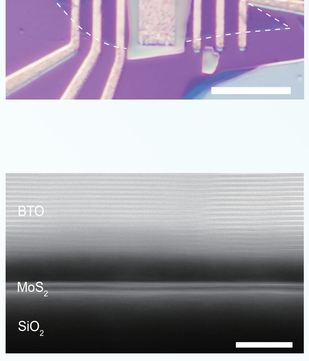




- Curling of ferroelectric freestanding BTO integrated by standard transfer

Anti-curling vdW integration strategy

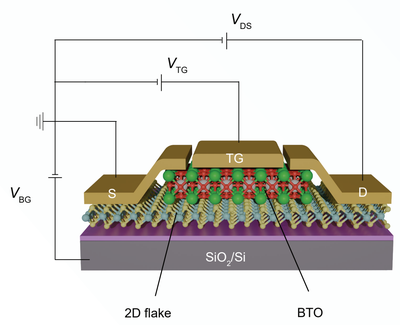


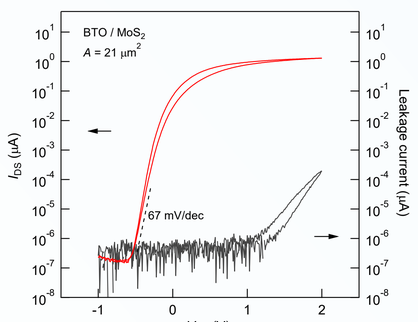


- We developed an anti-curling fabrication approach that combines three key steps: water-mediated release, PMMA-assisted transfer, and metal electrode confinement.

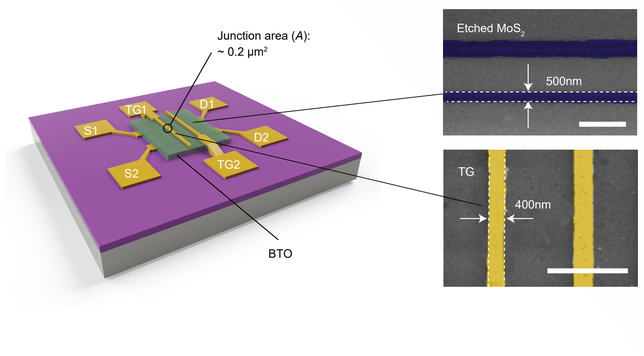
II. Nanoscale Junctions for Leakage Mitigation

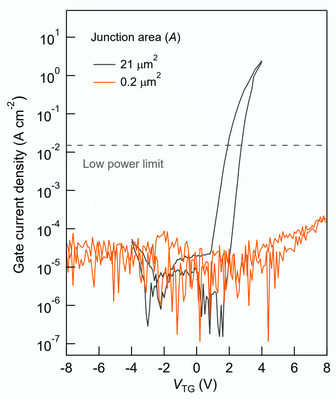
BTO top-gated FET with leakage current





Defect-tolerant miniaturized junction design

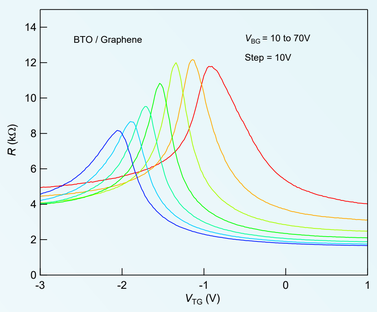


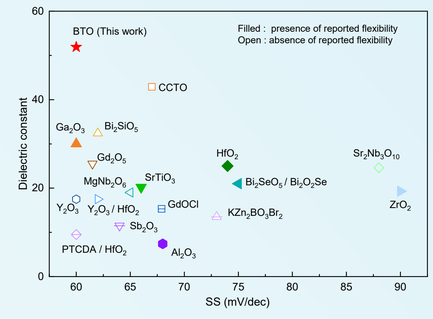


- This defect-tolerant miniaturized design diminishes leakage current, leading to an extended gate-voltage operating range.

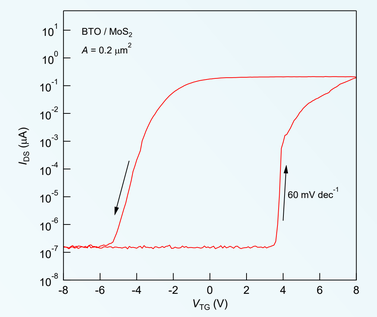
III. Device Characteristics of Top-gated Transistors

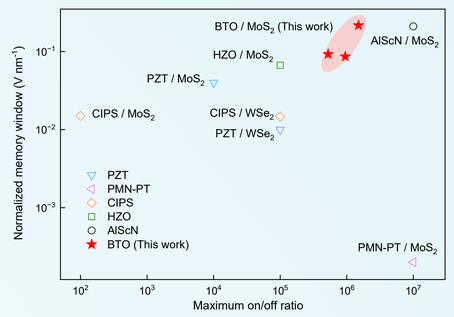
High dielectric constant





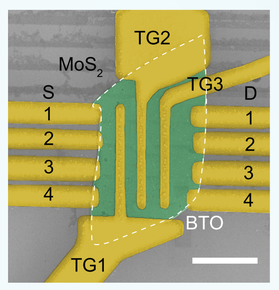
High-performance FeFET

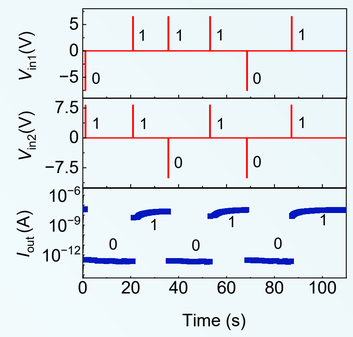




IV. FeFET Array with Memory and Synaptic Capabilities

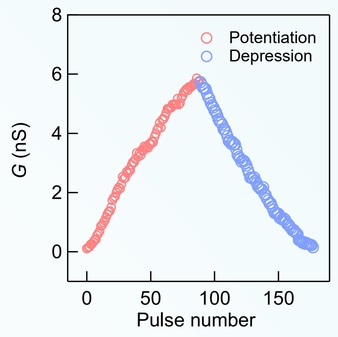
A prototype FeFET array with nonvolatile logic operation

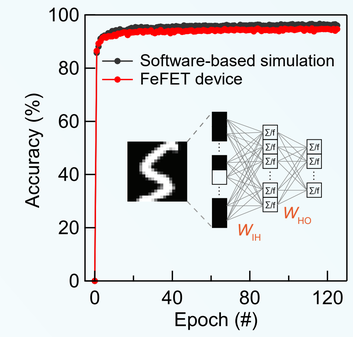




Synaptic operations

- A simple AND gate logic operation





- Synaptic weight update characteristics of a typical FeFET memory cell

Conclusion

- Developed anti-curling integration and realized uniform vdW interface
- Mitigated leakage current and realization of FeFETs with superior device metrics
- Demonstrated FeFET arrays with in-memory logic and synaptic functionalities

Reference & Contact

Z.Guo, X.Sha, F.Xu, et al. Advanced Science.13, no. 12 (2026): e20610

Contact: zjguo23@m.fudan.edu.cn; shiwu@fudan.edu.cn